Am79C411 CT2 PhoX[™] Controller for Digital Cordless Telephones Technical Manual

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OVERVIEW

1.1 GENERAL DESCRIPTION

The Am79C411 is an addition to AMD's PhoX[™] Controller family of CT2 devices, providing an integrated baseband solution for the CAI CT2 (Common Air Interface, Cordless Telephone, Second Generation) digital cordless telephone standard described by ETSI document I-ETS 300 131. The Am79C411 integrates the baseband functions required by CT2 telephone basestations in a single chip, including protocol control, ADPCM transcoding, serial PCM I/O, and peripheral functions. Figure 1-1 shows the basic building blocks of the PhoX controller.

Local radio link control can be executed from the on-chip 8051-class microcontroller, reading from an external program ROM. The controller can perform CT2 layer 3 and partial layer 2 functions and drive the hardware that performs the partial layer 2 and layer 1 functions. It initializes the audio path and services the various on-chip peripherals. The PhoX controller can respond to higher level system control through its asynchronous serial port.

In Emulation mode, the microcontroller is bypassed for direct control of the device from an external controller. For software development, the chip interfaces directly to standard 8051 in-circuit emulators.

The Am79C411 CT2 Formatter performs all the CT2 protocol requirements as well as baseband transmission and reception under control of the on-chip microcontroller. CT2 telephones use a 32-kbps voice (B) channel and a 1-, 2-, or 16-kbps control (D) channel between the handset and the base station. The physical implementation is a 72-kbps time-division duplex radio link with identical transmit and receive frequencies in the 864-to 868-MHz range. Software controls the contents of the D channel and the device performs the basic functions of packetizing the data and evaluating the check fields. The B channel is an ADPCM (Adaptive Differential Pulse Code Modulation) compressed data stream. The PhoX chip translates transparently between ADPCM and 64-kbps A-law or μ -law PCM. The device also provides digitally generated DTMF (Dual-Tone Multi-Frequency) tones.

Programmable radio control timing will accommodate a variety of radio designs. Transmission can be synchronized to an externally provided 500-Hz timing signal.

Baseband transmit data is filtered on-chip to provide analog I/Q Gaussian minimum-shift key (GMSK) output meeting CT2 spectral requirements. GMSK is a form of frequency shift keying modulation that minimizes bandwidth by conditioning the pulse shapes of the individual transmitted data bits. Data is also available unfiltered in a pseudo-digital NRZ format.

The Am79C411 PhoX controller incorporates other peripheral functions necessary for digital cordless telephones. For example, it has an A/D converter for the receive signal strength indicator (RSSI) measurement and a serial port for interfacing with synthesizers and EEPROMs. The chip also includes several multifunction ports.

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Figure 1-1 Basic Chip Architecture



Figure 1-2 demonstrates an application of the Am79C411 in a multichannel base station cluster. The architecture assumes a remote centralized digital control and switching entity. All PhoX devices in the cluster are slaved to a 500-Hz synchronization clock for optimal radio performance. Control information is passed through the asynchronous serial port and the traffic channel is conducted over a serial PCM link.

Figure 1-2 System Architecture Example



CT2 CAI Licensing

The Am79C411 PhoX device has applications in CT2 cordless telephones and other digital wireless systems. Purchasers of these devices should be aware that the Common Air Interface Founders Group holds patents in many countries covering such applications. The Founders Group has stated its intention to grant royalty-free licenses to system manufacturers wishing to produce CT2 products, subject to certain territorial restrictions. Other applications may also require licenses. For information concerning CT2 applications, interested parties should contact:

Secretariat, Common Air Interface Founders Group Lingdales, Glendyke Road Liverpool L18 6JR, United Kingdom Tel: +44-51-724 5591 Fax: +44-51-724 6938 1.2

DISTINCTIVE CHARACTERISTICS

- The Am79C411 CT2 PhoX controller performs all protocol, data formatting, digital signal processing, and peripheral functions for the Common Air Interface, Cordless Telephones, Second Generation (CAI CT2) all-digital base stations.
- The on-chip 8051-class microcontroller controls all functions.
- Special CAI CT2 features are:
 - Link controller that performs all data transmission and reception
 - Flexible radio controls
 - Baseband I/Q GMSK modulator that conforms to CAI CT2 transmission spectrum requirements
 - Selectable output drive format, I/Q or NRZ
 - Receive signal strength indicator for channel scanning
 - CT2 frame synchronization port
- Special digital audio processing features are:
 - ADPCM transcoder compliant with CCITT G.721
 - A-law or μ-law PCM serial port
 - Dual-Tone Multi-Frequency (DTMF) generator
- Other on-chip peripheral functions include:
 - Serial port for synthesizer, EEPROM, and LCD
 - Up to 9 general-purpose output ports
 - Watchdog timer
- Built-in power management features are:
 - Single 3-V or 3- to 5-V supply
 - Low active power consumption, 38 mW
 - Super low power shutdown mode, 108 μW
- Test and development features are:
 - In-circuit 8051 emulator support for code development
 - Numerous test paths and loopbacks for bit error rate, continuity, and performance testing
 - Continuous transmit RF spectral measurement and modulator bypass features
- The device is packaged in a 100-pin plastic quad flat pack (PQFP).





Figure 1-4 Connection Diagram

Top View



Note:

Pins denoted as NC (No Connection) are reserved and should not be externally connected or used as circuit routing channels.

1.3 PIN LIST

Pin	Pin Name	Default Function (multifunction pins) or 80C32T2 Port Special Function	Alternate 1 (multifunction pins)	Alternate 2 (multifunction pins)	Alternate 3 (multifunction pins)
1–6	NC				
7	OUT6				
8	OUT7				
9	BDP5_OUT11	TXENCIN	OUT11		
10	TRI0_OUT10	TRI0	OUT10		
11	BDP4_OUT8	RXENCOUT	OUT8		
12	BDP3_OUT5	CLK8K	OUT5	DTXCLK	CLK8K
13	DVss				
14	BDP2_OUT4	BCLK	OUT4	DRXCLK	CT2TXEN
15	BDP1_OUT3	BCHIN	OUT3	DTXDATAIO	CT2TXCLK
16	BDP0_OUT2	BCHOUT	OUT2	DCT2RX	CT2TXD
17	SHCTR				
18	DVss				
19	TXPWR				
20	DVcc				
21	P1.0				
22	P1.1				
23	P1.2				
24	P1.3				
25	P1.4				
26	P1.5				
27	P1.6	P1.6	SYNC		
28	P1.7				
29	PSEN				
30	P3.0	RXD			
31	P3.1	TXD			
32	P3.6	WR			
33	P3.7	RD			
34	CS2_CPUCLK	CS2	CPUCLK		
35	ALE	ALE			
36	P2.0	A[8]			
37	P2.1	A[9]			
38	P2.2	A[10]			
39	P2.3	A[11]			
40	P2.4	A[12]			

Pin	Pin Name	Default Function (multifunction pins) or 80C32T2 Port Special Function	Alternate 1 (multifunction pins)	Alternate 2 (multifunction pins)	Alternate 3 (multifunction pins)
41	P2.5	A[13]			
42	P2.6	A[14]			
43	P2.7	A[15]			
44	P0.0	A/D[0]			
45	P0.1	A/D[1]			
46	P0.2	A/D[2]			
47	P0.3	A/D[3]			
48	P0.4	A/D[4]			
49	P0.5	A/D[5]			
50	P0.6	A/D[6]			
51	DVcc				
52	P0.7	A/D[7]			
53	DVss				
54	CS0_INT0	CS0	ĪNT0		
55	CS1_INT1	CS1	INT1		
56	DVss				
57	NC				
58	PCMIN				
59	PCMOUT				
60	PCMCLK				
61	RE				
62	TE				
63	CLK4M				
64	DVss				
65	DVss				
66	NC				
67	DVcc				
68	MXTAL1				
69	MXTAL2				
70	SCLK				
71	SDIN				
72	SDOUT				
73	CT2RX				
74	XINT0				
75	XINT1				
76	XINT2_ANTSW	XINT2	ANTSW		
77	TRI1				

Pin	Pin Name	Default Function (multifunction pins)	Alternate 1 (multifunction pins)	Alternate 2 (multifunction pins)	Alternate 3 (multifunction pins)
78	TXEN				
79	RXEN				
80	RESET				
81	AVss				
82	RSSI				
83	ТХІ	ТХІ	NRZ+		
84	MREF				
85	TXQ	TXQ	NRZ–		
86	AVcc				
87	NC				
88	AVss				
89	NC				
90	NC				
91	NC				
92	NC				
93	AVss				
94	CFILT				
95	IREF				
96	AVcc				
97	NC				
98	NC				
99	NC				
100	NC				

1.4 LOGIC SYMBOL

				7
	MXTAL1		BDP0_OUT2	├
•	MXTAL2		BDP1_OUT3	← →
	DESET		BDP2_OUT4	├
	REGET		BDP3_OUT5	→
	DVcc		BDP4_OUT8	├
	DVss		BDP5_OUT11	← →
	AVcc			
	AVss		PSEN	→
•	IREF		P0.7-P0.0	← →
◀	CFILT		P1.7–P1.0	← →
	тс	Am79C411	P2.7-P2.0	← →
	RE		P3.7–P3.6	••
	PCMCLK		P3.1–P3.0	←
	PCMIN			
•	PCMOUT		CS0_INT0	
	XINTO		CS1_INT1	
	XINT1		CS2_CPUCLK	├ →
← →	XINT2 ANTSW		ALE	←
	TRI1			
			RXEN	├ →
>	SDIN		SHCIR	
•	SDOUT			
•	SCLK		CLK4M	
	CT2RX		TXI	
	RSSI		TXQ	
			MREF	

1.5 ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (valid combination) is formed by a combination of the elements below:



Am79C411 CT2 PhoX Controller for Digital Cordless Telephones

Valid Combinations			
	LKC		
AN700411	XKC		
AW179C411	ХКТ		
	XKI		

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's extended temperature range products.

Note:

1. Standard product is available in the PQR 100 trimmed and formed package. Special requests may be made to the local AMD sales office for samples in the PQR 100 package with a protective carrier ring package.

1.6 PIN DESCRIPTION

All signals are CMOS levels unless otherwise stated. A ♦ indicates multifunction pins whose characteristics depend on software configuration and that may appear in more than one of the following tables. See Section 1.7 Am79C411 Pin Multiplexing for a summary of multifunction pins.

1.6.1 CT2 Pins

Pin #	Pin Name	l/O Type	Description	
63	CLK4M	0	4.608-MHz 50% duty cycle clock output.	
16	BDP0_OUT2	• 0	Digital B or D channel output or clock. In shutdown mode, the pin retains its value.	
15	BDP1_OUT3	♦I/O	Digital B channel input, D channel I/O, B+D transmit data (CT2TXD signal) or modulator test data input. As an output in shutdown mode, the pin retains its value.	
14	BDP2_OUT4	•0	Digital B or D channel clock output. In shutdown mode, the pin retains its value. Also the CT2TXEN pulse, which is active during transmission when properly configured.	
12	BDP3_OUT5	• 0	Digital B or D channel clock output. In shutdown mode, the pin retains its value.	
73	CT2RX	Ι	72-kHz digital receive data with CMOS levels. Not internally Schmitt triggered.	
84	MREF	0	Modulator DC reference. $0.5 \times Vcc\pm 5\%$. When disabled, the pin looks like a 25-k Ω resistance to analog ground.	
27	P1.6	♦I/O	CT2 500-Hz SYNC input.	
82	RSSI	I	Receive signal strength indicator analog input. High imped- ance, DC coupled. For noise rejection, a small filter capacitor may be tied between RSSI and analog ground.	
79	RXEN	0	Active High strobe indicating CT2 receive window for enabling receiver IF and RF circuits.	
17	SHCTR	0	Sample/hold control for maintaining receiver discriminator DC level between receive windows.	
78	TXEN	0	Active High strobe indicating CT2 transmit window for enabling transmitter IF and RF circuits.	
83	ТХІ	0	Modulator in-phase output. ± 0.5 -V peak, DC coupled, inter- nally DC biased to MREF. Also NRZ+ output. When disabled, the pin looks like a 25-k Ω resistance to analog ground.	
19	TXPWR	0	Normal/low power transmitter mode or antenna diversity con- trol output.	
85	TXQ	0	Modulator quadrature output. ± 0.5 -V peak, DC coupled, internally DC biased to MREF. Also NRZ+ output. When disabled, the pin looks like a 25-k Ω resistance to analog ground	
76	XINT2_ANTSW	♦ I/O	Antenna Switch RF Timing control output.	

1.6.2 Audio Pins

Pin #	Pin Name	l/O Type	Description	
16	BDP0_OUT2	• 0	32-kbps ADPCM B channel output. In shutdown mode, the pin retains its value.	
15	BDP1_OUT3	♦I/O	32-kbps ADPCM B channel input.	
14	BDP2_OUT4	♦ 0	Digital B channel bit clock output. In shutdown mode, the pin retains its value.	
12	BDP3_OUT5	• 0	Digital B channel frame clock output. In shutdown mode, the pir retains its value.	
11	BDP4_OUT8	♦ 0	 O Digital B channel encryption output. In shutdown mode, the pretains its value. 	
9	BDP5_OUT11	♦I/O	Digital B channel encryption input.	
60	PCMCLK	I	Serial PCM port clock input.	
58	PCMIN	I	Transmit A-law or μ-law input data	
59	PCMOUT	0	Receive A-law or μ-law output data	
61	RE		Receive PCM strobe input for A-law or µ-law PCM.	
62	TE	I	Transmit PCM strobe input for A-law or μ -law PCM.	

1.6.3 Microcontroller and Address Decoder Pins

Pin #	Pin Name	l/O Type	Description	
35	ALE	♦I/O	The ALE signal is the 80C32T2 address latch enable for latching the lower order address on the P0 bus during external accesses. In Emulation mode, the pin is the ALE input for addressing on-chip memory and registers.	
54	CS0_INT0	♦ 0	♦O In normal mode, CSO_INTO drives the CSO output, an active Low address space decode. In Emulation mode, it drives the INTO signal, which is ordinarily connected to the 8051 emulato INTO input.	
55	CS1_INT1	• 0	In normal mode, CS1_INT1 drives the CS1 output, an active Low address space decode. In Emulation mode, it drives the INT1 signal, which is ordinarily connected to the 8051-emulator INT1 input.	
34	CS2_CPUCLK	• 0	This multifunction pin is configured by software and Emulation mode selection to be either the $\overline{CS2}$ address space decode output or the 80C32T2 clock output.	
44–50, 52	P0.7–P0.0	I/O	Port 0 is the multiplexed data and lower order address bus for external data and program memory access, using strong internal pull-ups when driving 1s. See Appendix B.5 for detailed information.	
			P0.7–P0.0 are held weakly High during reset. In shutdown mode, they are held strongly Low or weakly High, depending on the last operation performed on them. They are high impedance in Emulation mode.	

Microcontroller Pins (continued)

Pin #	Pin Name	l/O Type	Description	
21–28	P1.7–P1.0	I/O	 Port 1 is an 8-bit I/O port with internal pull-ups. Port 1 pins written to 1s are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins externally pulled Low source current because of the pull-ups. All Port 1 pins may be programmed to generate interrupts in response to changes of state. Port 1 pins configured to drive 1s actively drive a High level for only two clock cycles, after which they are weakly held High by internal pull-ups. P1.7–P1.0 are held weakly High during reset and retain their programmed values in shutdown mode. They are high impedance in Emulation mode. The pull-up associated with each pin can be individually disabled. 	
36–43	P2.7–P2.0	I/O	Port 2 is the upper order address byte during fetches from pro- gram memory and during access to external data memory that use the MOVX @DPTR instruction. In this application, it uses strong pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 special function register. P2.7–P2.0 are held weakly High during reset and in shutdown mode and are high impedance in Emulation mode. The pull-up associated with each pin can be individually dis- abled	
30 31	P3.1–P3.0	I/O	Ports P3.1 and P3.0 are I/O ports with internal pull-ups. When written to 1s they are pulled High by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins externally pulled Low source current because of the pull-ups. The pull-up asso- ciated with each pin can be individually disabled.The pins also serve the functions of the special features listed below.Port PinAlternate FunctionP3.0RxD (serial input port)P3.1TxD (serial output port)	
32	P3.6	I/O	The P3.6 pin is the \overline{WR} signal, which is the active Low external data memory write strobe. In normal mode, P3.6 is the \overline{WR} output for external components. In Emulation mode, it is the \overline{WR} input for writing on-chip memory and registers.	
33	P3.7	I/O	The P3.7 pin is the \overline{RD} signal, which is the active Low external data memory read strobe. In normal mode, P3.7 is the \overline{RD} output for external components. In Emulation mode, it is the \overline{RD} input for reading on-chip memory and registers.	
29	PSEN	0	PSEN is the active Low read strobe to external program memory.In shutdown PSEN is held weakly High. In Emulation mode, thepin is high impedance.	

1.6.4 Parallel Port and Serial Port Pins

Pin #	Pin Name	l/O Type	Description	
16 15 14 12 7 8 11 9	BDP0_OUT2 BDP1_OUT3 BDP2_OUT4 BDP3_OUT5 OUT6 OUT7 BDP4_OUT8 BDP5_OUT11	 ♦ O ♦ I/O ♦ O ♦ O ♦ O 0 ♦ O ♦ O	General-purpose outputs OUT[11, 8–2] are functions that share configurable multifunction pins. When programmed for the OUT function, the pin drives the level programmed in the associated GPOCTR0 or GPOCTR1 register and retains that value when the chip goes into shutdown mode. Outputs default to 1 at reset.	
10	TRI0_OUT10	♦ I/O	TRI0_OUT10 is a multifunction pin configured to provide the TRI0 input or the OUT10 output. As TRI0, it is a software read- able three-level input detecting Vss, Vcc, and open (no con- nect). As OUT10, it is driven to the state programmed by soft- ware in the GPOCTR1 register.	
77	TRI1	I	Three-level software readable input: Vss, Vcc, and open (no connect). During reset, the state on TRI1 determines whether the chip is in Emulation mode.	
74	XINT0	I	External Interrupt 0 generates an interrupt on a change of state.	
75	XINT1	I	External Interrupt 1 generates an interrupt on a change of state.	
76	XINT2_ANTSW	♦I/O	External Interrupt 2 generates an interrupt on a change of state.	
70	SCLK	• 0	Synchronous serial port clock output function. It is pulled Low when the serial port is disabled or when the chip is in shutdown.	
71	SDIN	♦I	Synchronous serial port data input function.	
72	SDOUT	♦ 0	Synchronous serial port data output function. The pin is pulled Low when the serial port is disabled or when the chip is in shutdown.	

1.6.5 Crystal, Reset, and Power Supply Pins

Pin #	Pin Name	l/O Type	Description	
86 96	AVcc	Ι	 Analog power supply, which must be connected to the digital power supply. It is important to provide decoupling capacitors of ≈1 μF across the following pin combinations: decouple pin 86 to ground pin 81 (modulator and RSSI supply) decouple pin 86 to ground pin 88 decouple pin 96 to ground pin 93 	
81 88 93	AVss	0	Analog ground. Analog and digital grounds must be connected.	
94	CFILT	0	$0.32 \times Vcc$ DC bias filter pin. Must be connected to an $11-\mu F$ capacitance ($10-\mu F$ low-frequency capacitor in parallel with $1-\mu F$ high-frequency capacitor) tied to ground and located close to the IC to minimize noise. The pin is not disabled by shutdown or reset.	
20 51 67	DVcc	1	 Digital power supply. Digital and analog supplies must be tied together. It is important to provide decoupling capacitors of ≈0.1-µF across the following pin combinations: decouple pin 20 to ground pin 18 decouple pin 51 to ground pin 53 decouple pin 67 to ground pin 13 decouple pin 67 to battery ground pin 64 	
13 18 53 56 64 65	DVss	0	Digital ground. Digital and analog grounds must be connected.	
95	IREF	0	Current reference output, which must be tied to a temperature stable resistor connected to analog ground and located as close as possible to the IC to minimize noise. The resistor should be 61.9 k Ω with 1% tolerance, creating a ~20- μ A reference. The pin goes to high impedance in shutdown mode.	
68	MXTAL1	I	18.432-MHz crystal input. A 2-Vpp digital clock, AC coupled through 30 pF, may be used.	
69	MXTAL2	0	18.432-MHz crystal output. If a digital clock input is used, this pin should be pulled up to DVcc through a 2.2-k Ω resistor.	
80	RESET	I/O	Active Low, open-drain reset input returns chip to default state. The pin must be externally pulled up. Watchdog timer function drives the pin Low when timer expires. In Emulation mode, the pin is an input only.	

1.7 Am79C411 PIN MULTIPLEXING

The Multifunction Pin Summary lists multifunction pins and their function selection controls.

Pin Name	Pin	Multiplexed Functions	Function Selection	Page
BDP0_OUT2	16	 32-kbps B channel output general-purpose output port 2 receive D channel monitor data 72-kHz CT2 clock output 	BDMUX[6:5]	2-36, 2-39 2-11 2-41 2-24
BDP1_OUT3	15	 32-kbps B channel input general-purpose output port 3 transmit D channel data I/O 72-kHz CT2 digital data output Modulator test data input 	BDMUX[6:5], DEVTEST	2-36, 2-40 2-11 2-41 2-24 2-39
BDP2_OUT4	14	 14 • 32-kHz B channel clock out • general-purpose output port 4 • receive D channel monitor clock • 500-Hz CT2 transmit window 		3-36, 2-40 2-11 2-41 2-24
BDP3_OUT5	IT5 12 • 8-kHz B channel output BDMUX[6:5] • general-purpose output port 5 • transmit D channel I/O clock		2-36, 2-40 2-11 2-41	
BDP4_OUT8	11	32-kbps encryption outputgeneral-purpose output 8	BDMUX[7]	3-12, 2-36 2-11
BDP5_OUT11	9	32-kbps encryption inputgeneral-purpose output 11	BDMUX[7]	3-12, 2-36 2-11
CS0_INT0	54	 chip select output 0 INTO interrupt output 	Emulation mode	2-6 2-38
CS1_INT1	55	 chip select output 0 INT1 interrupt output 	Emulation mode	2-6 2-38
CS2_CPUCLK	34	 chip select output 2 80C32T2 clock output	Emulation mode ADRDEC[1]	3-3, 2-6 2-38
P1.6	27	 8032 port P1.6 CT2 500-Hz SYNC I/O	BSYNC, P1SRC2[6]	3-41, B-8 2-14
TRI0_OUT10	10	• 3-level input 0 • general-purpose output 10 GPOCTR1[7]		3-9 2-11
ТХІ	83	In-phase modulator output MODTST[4] NRZ+ output		3-18 2-30
TXQ	85	Quadrature modulator output MODTST[4] NRZ– output		3-18 2-30
XINT2_ANTSW	76	 External Interrupt Input ANTSW antenna switch output 	RDELAY[5]	3-43, 2-11 2-24

1.8 GLOSSARY OF TERMS

The following terms are used frequently throughout the text:

ADPCM	Adaptive Differential Pulse Code Modulation, a voice compression and encoding technique
B Channel	Voice Channel, 32 kbits
CAI	Common Air Interface
CCITT	International Telegraph and Telephone Consultative Committee
CFP	Cordless Fixed Part (basestation)
CHM (CHMF, CHMP)	Channel Marker. Suffixes F and P refer to Fixed parts and Portable parts (CFP and CPP)
CPP	Cordless Portable Part (handset)
CRC	Cyclic Redundancy Check
CT2	Cordless Telephone, Second Generation
D Channel	Control Channel
DTMF	Dual-Tone Multi-Frequency
ETSI	European Telecommunications Standards Institute
GMSK	Gaussian Minimum-Shift Key
IDLE_D	D Channel Idle fill pattern
MUX	Multiplex, a time-division duplex structure
NRZ	Non-Return-To-Zero
PCM	Pulse Code Modulation, a logarithmic encoding technique
PLL	Phase-Locked Loop
POTS	Plain Old Telephone Service (i.e., standard analog line service)
PSTN	Public Switched Telephone Network
RSSI	Receive Signal Strength Indicator
SFR	8032 Microcontroller Special Function Register
SYN Channel	Synchronization Channel
SYNC (SYNCF, SYNCP)	Synchronization Pattern. Suffixes F and P refer to Fixed and Por- table parts (CFP and CPP)
SYNCD	D Channel Synchronization pattern



FUNCTIONAL DESCRIPTION

2.1 GLOBAL FUNCTIONS

2.1.1 Reset and Basic Mode Establishment

The reset pin is an active Low I/O that resets the chip to its default state when driven Low. The chip drives reset Low due to watchdog timer expiration or software reset. A software reset may be induced by writing 00 hex to the WDTKEY register.

The basic operating mode is defined by the level of the TRI1 pin during reset, according to Table 2-1.

Table 2-1 Establishing the Basic Operating Mode

Basic Operating Mode	TRI1 Pin During Reset		
Normal Mode	Vcc		
Customer Test Mode	Unconnected		
Emulation Mode	Vss		

Normal mode is for typical application of the chip. Customer test mode is functionally the same as normal mode, but provides for software branching to test routines, such as factory built-in test features, based on the read value of the TRI1 register. Emulation mode is for code development with an 8051 in-circuit emulator.

2.1.2 Power Management and Shutdown Mode

The power management features of the PhoX chip are centralized in a block called the clock generator. The MXTAL1 and MXTAL2 pins connect to an 18.432-MHz crystal oscillator. Each functional block in the chip is individually enabled or disabled by programming the appropriate bit in the MECTR0 or MECTR1 register.

The shutdown state disables all synchronous and analog circuits, including the main oscillator, minimizing power consumption. Programming UCCCTR[7] initiates the shutdown sequence, which brings the PhoX chip cleanly to a static state. The shutdown sequence takes 3.56 to 7.2 ms to complete depending on the initial conditions, so software has 3.56 ms to perform housekeeping tasks necessary before all clocks on the chip stop and analog circuits power down. These tasks should include programming the 80C32T2 for idle mode. Any enabled interrupt occurring during the sequence will cause it to abort.

Any enabled interrupt awakens the chip from shutdown. The wake-up sequence takes 3.56 ms, as determined by counting 18.432-MHz crystal periods, and returns the PhoX chip to its condition before shutdown. The measured wake-up sequence time will vary with actual crystal start-up and stabilization times. Analog circuits take approximately 300 μs to reactivate and stabilize.

The 80C32T2 clock rate is programmable in the UCCCTR register for reduced power consumption. The clock rate control mechanism includes an automatic speed-up feature, which allows any interrupt to increase the clock rate immediately to maximum speed for

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fast interrupt service. When enabled, auto speed-up responds to interrupts on the 8032 $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ interrupts. These interrupts are internal to the chip and are driven by the interrupt controller.

2.2 SYSTEM CONTROL BLOCK FUNCTIONS

2.2.1 80C32T2 Microcontroller

The microcontroller in the PhoX chip is a member of the 8051 family of microcontrollers, with the standard 8051-family architecture and instruction set. While it is substantially identical to the PhoX Controller 8032, some enhancements have been made to meet the special needs of the CT2 environment. Despite these differences, the microcontroller is referred to throughout this data book as an 80C32T2 or simply 8032. A key feature of the PhoX Controller 8032 is its dual data pointer. Appendices B, C, and D define the architecture, programming requirements, and instruction set for the 8032.

2.2.1.1 Memory

Program Memory Map:

Program Space	Address Range	Size
External ROM	0000–FFFF	64 Kbyte

Data Memory Map:

8032 Internal Data Space (access by mov)	Address Range	Size
Internal RAM,	00–7F	128 byte
direct/indirect access		
Internal RAM,	80–FF	128 byte
indirect access only		
Special Function Registers (SFRs)	80–FF	27 byte

8032 External Data Space (access by movx)	Address Range	Size
I/O 1	0000-EFFF	60 Kbyte
I/O 0	F000–F3FF	1 Kbyte
I/O 2	F400–F7FF	1 Kbyte
(unmapped)	F800–FEFF	2 Kbyte
PhoX Chip Memory Mapped Registers	FF00-FFFF	256 byte

2.2.1.2 Clock Input

The microcontroller is clocked by an internal signal called CPUCLK, which is derived from the MXTAL1 and MXTAL2 pins. The frequency of CPUCLK is programmable from 72 kHz to 9.216 MHz in the UCCCTR register. By programming UCCCTR for shutdown mode, CPUCLK stops entirely. The automatic speed-up mode enables hardware to immediately increase the CPUCLK speed to its maximum when triggered by an interrupt at either of the 8032 external interrupts, INTO or INT1. The auto speed-up feature does not respond to the 8032 timer/counter or serial port interrupts.

2.2.1.3 **RESET** and **EA**

The reset input is active Low, different from the standard 8051-family microcontroller reset inputs. The PhoX chip has no external address select (\overline{EA}) pin present in standard 8051-family microcontrollers because it has no internal program ROM.

2.2.1.4 Microcontroller Port Modifications

The microcontroller ports support CMOS levels. When the device is in Emulation mode, ports assume a high-impedance state.

In order to eliminate spurious glitches during reset, all ports are driven to the float high condition during reset.

To minimize power consumption, the Port 1, 2, and 3 buffers are capable of disabling the weak pull-ups by software control of the Port Control Register Bit special function registers.

2.2.1.5 SFR Map Additions

The special function registers listed in Table 2-2 are added to the standard 8032 SFR map to disable microcontroller port pin weak pull-ups. SFRs marked with * can be accessed only when PCFIG[0] has been set High.

SFR Name	SFR Address	SFR default after Reset
PCFIG	A1H	00H
P1PCRB	90H *	00H
P2PCRB	A0H *	00H
P3PCRB	B0H *	00H

Table 2-2 SFR Additions

Note:

* = These SFRs can be accessed only when PCFIG[0] has been set High.

Each P_x PCRB (Port [1,2,3] Port Control Register Bit) SFR contains 8 bits corresponding to the 8 bits in each of the P1, P2, and P3 ports. When a P_x PCRB bit is cleared, the associated port behaves as a standard 8032 port, where an internal weak pull-up is applied to a port driving a 1. Setting a P_x PCRB bit disables the weak pull-up in the respective port bit, making it a high-impedance input port when the port SFR is programmed to 1.

Notice that the P*x*PCRB SFRs share the same address as the port SFRs. PCFIG is a 1-bit register, and bit PCFIG[0] selects access to either the port SFR or the P*x*PCRB SFR. PCFIG[0] must be set to access the P*x*PCRB registers and must be cleared to access the port SFRs.

2.2.1.6 **PSEN** Modifications

To reduce power consumption during instruction fetches from external program ROM, the $\overrightarrow{\text{PSEN}}$ pulse width is reduced when the CPUCLK clock signal is programmed below 9.216 MHz.

2.2.1.7 Interrupt Modifications

The INTO (P3.2) and INT1 (P3.3) interrupt inputs are driven internally. The interrupt sources on the PhoX chip, reported in the MISRC0 and MISRC1 registers, are fundamentally level-sensitive in nature. Therefore, TCON[2,0] should be programmed Low for proper interrupt response.

The 8032 IDLE mode (PCON[0]) supports the low-power shutdown mode such that the controller clock can be stopped indefinitely. To avoid the possibility of entering IDLE with all interrupts disabled and therefore being incapable of awakening from IDLE mode without a full reset, the 8032 ignores the interrupt mask bits IE[7,2,0] when in IDLE mode. Both external interrupts are enabled but the IE bits themselves are unchanged.

For software development purposes in the in-circuit emulator environment, software should always enable interrupts in IE before programming IDLE, since the wakeup safeguard is not present in standard 8051-family emulators.

2.2.1.8 T0 and T1

The T0 (P3.4) and T1 (P3.5) signals do not appear as pins on the PhoX chip. They are internally tied to a 18-kHz clock source enabled in the MECTR0 register, located in external data space.

The user should be aware that there are operational restrictions on the CPUCLK rate when the T0 and T1 timers are used in the counter mode. In counter mode, the 8032 samples the T0 and T1 inputs once per machine cycle and increments the counter only on negative transitions of the sampled counter input; therefore, the counter function works normally only for CPUCLK rates greater than 24×18 kHz (i.e., 576 kHz to 9.216 MHz).

2.2.2 Interrupt Controller

The centralized interrupt controller incorporates all interrupts generated by the various on-chip functions into the INTO and INT1 interrupts recognized by the 8032 microcontroller. Software controls masking in the MIMSK0 and MIMSK1 registers and determines interrupt sources by reading status registers MISRC0 and MISRC1. Figure 2-1 shows the interrupt tree. For proper response to all interrupts, the 8032 should be programmed for level-sensitive interrupts. Tables 2-3 and 2-4 list all interrupt sources and service requirements.

Any unmasked interrupt causes a PhoX device in shutdown to awaken.

Figure 2-1 Interrupt Tree



Table 2-3 8032 INTO Interrupt Sources

MISRC0 Bit	Interrupt Mnemonic	Source	Description
0	DRXFULL	CT2 Formatter	D channel receive buffer full or half full. Cleared by reading RXBUF[0:5].
1	DRXERR	CT2 Formatter	CRC, parity, or overflow error detected in received D channel. Cleared by reading DCHSTAT.
2	DTXEMPTY	CT2 Formatter	D channel transmit buffer empty or half empty. Cleared by writing TXBUF[0:5] buffer.
3	EXTINT1	Parallel Port	A transition on the XINT1 pin has occurred. Cleared by reading XISTAT1.
4	EXTINT2	Parallel Port	A transition on the XINT2_ANTSW pin has occurred. Cleared by reading XISTAT2.
5	JITTER	Noise Suppression	Jitter or B Channel noise on received CT2 data exceeds programmed threshold. Cleared by reading NSCTR.

Table 2-4 8032 INT1 Interrupt Sources

MISRC1 Bit	Interrupt Mnemonic	Source	Description
0	EXTINT0	Parallel Port	A transition on the XINT0 pin has occurred. Cleared by reading XISTAT0.
2	SIO	Serial Port	Transmit buffer empty or receive data available. Cleared by writing to the transmit buffer or reading from the receive buffer, respectively.
3	CHM/SYNC	CT2 Formatter	A CHM/SYNC interrupt has occurred, as reflected in the CMSSRC register. Cleared by reading CMSSRC.
4	P1INT0	Parallel Port	An unmasked event has occurred on P1.1–P1.0. Cleared by reading P1SRC0.
5	P1INT1	Parallel Port	An unmasked event has occurred on P1.3–P1.2. Cleared by reading P1SRC1.
6	P1INT2	Parallel Port	An unmasked event has occurred on P1.7–P1.4. Cleared by reading P1SRC2.

2.2.3 Address Decoder

The address decoder decodes the 8032 external data spaces listed as $\overline{CS0}$ (Chip Select 0, active Low), $\overline{CS1}$, and $\overline{CS2}$ in Table 3-1. The active Low signals are present on multifunction pins $\overline{CS0}$ _INT0, $\overline{CS1}$ _INT1, and $\overline{CS2}$ _CPUCLK, respectively, when enabled in the ADRDEC register. The pins are automatically reconfigured in Emulation mode to provide the alternate functions, so the chip selects are not available. They can be easily regenerated externally, however, with standard decode logic.

2.2.4 Watchdog Timer (WDT) and Software Reset

Software must perform the watchdog timer (WDT) key sequence uninterrupted at least once every 1.82 seconds. Failure to correctly perform the key sequence results in a 1.78-ms output pulse on the reset pin and returns the device to its default condition. The key sequence is:

write WDTKEY= A5 hex write WDTKEY= 5A hex

It is recommended that interrupts be disabled while performing the watchdog timer sequence or that the timer be serviced in a high-priority interrupt routine that cannot be interrupted by another interrupt source.

Software may induce a software reset by writing WDTKEY=00. In fact, if any value is written to WDTKEY other than those listed in the key sequence, a reset results. Reset also occurs if the key sequence is incorrectly performed.

2.2.5 Serial Port

The serial port is a synchronous peripheral residing in 8032 external data space and is not the same as the 8032 serial interface. It provides a clean interface to popular serial EE-PROMs, LCDs, and synthesizers and performs two functions:

- 1. serial output only
- 2. serial output followed by input

Programmable features include transmit and receive buffer lengths, clock rate, and clock polarity and are under the control of the SIOTLB, SIOTMG, and SIOMODE registers. Interrupts are enabled in the SIOMASK register and reported in the SIOSTAT and SIOSRC registers. Figures 2-2 through 2-6 demonstrate the various clock and data relationships programmable in the SIOMODE register.

Some serial devices require one additional bit of delay between transmit and receive data bits, which can be accommodated by programming the serial port to transmit one extra bit after the normal address field has been transmitted.

To service several serial devices, drive the serial device chip select controls with any of the software-controlled ports to avoid contention.

For power management, the serial port operates in enabled and disabled modes, according to MECTR0[4]. When disabled, the SCLK and SDOUT pins are pulled Low and the serial port interrupt is disabled.

Figure 2-2 Serial Port Write Only Timing Example



Figure 2-3 Serial Port Write/Read Timing Example 1



(Transmit Buffer Length = 4)

Figure 2-4 Serial Port Write/Read Timing Example 2







(Transmit Buffer Length = 3)

Serial Port Write/Read Timing Example 4 Figure 2-6


2.2.6 Parallel Port

The parallel port is a grouping of four independent functions: P1 interrupts, external interrupts, general-purpose output latches, and tri-level inputs.

- The P1 interrupt function recognizes events at the eight 8032 P1 port pins and generates maskable interrupts in response. An event may be either a positive or negative transition of a pin, which is programmed in the P1TRIG register. Bits are individually masked in the P1MASK register. Events are reported in the P1SRC0, P1SRC1, and P1SRC2 registers.
- Three external interrupt inputs are provided on the XINT0, XINT1, and XINT2_ANTSW pins. Any change of state on an XINT pin sets a latch causing an interrupt to appear in the interrupt controller MISRC0 or MISRC1 register. The interrupts are enabled in the MIMSK0 and MIMSK1 registers. Reading XISTAT0, XISTAT1, or XISTAT2, which report the current level of the pins, clears the respective interrupt. The XINT2_ANTSW pin also has a use as the RF antenna switch control, described in Section 2.3.1.12, and can therefore provide interrupts timed by the CT2 radio link.
- The nine general-purpose outputs drive their respective pins to values programmed in the GPOCTR0 and GPOCTR1 registers. Each output uses a multifunction pin and is available only when that pin is programmed for the general-purpose output function in the BDMUX or GPOCTR1 registers. Outputs are designed for high-current drive. For noise immunity under heavy load conditions, no more than four output levels should be changed at one time.
- The two tri-level inputs are the TRI1 and TRI0_OUT10 pins. TRI0_OUT10 is a multifunction pin and the TRI0 function is available only if GPOCTR1[7] is programmed to 0. Each input converts a three-level input (low, high, and mid-supply) to a 2-bit value in the XISTAT0 register. The pins are weakly driven to Vcc/2 during reads so that the mid-supply level results if the pin is not connected. The TRI1 pin determines the basic operating mode of the PhoX chip at reset as shown in Table 2-1. Reset initialization typically completes 3.56 ms after the rising edge of the active Low reset input pulse. The basic mode is not reevaluated after the reset initialization and TRI1 may be redefined by the user.

2.3 CT2 SPECIFIC FUNCTIONS

2.3.1 CT2 Formatter

2.3.1.1 Block Diagram

The CT2 Formatter provides full support of CT2 signaling layers one and two. It includes a synchronization (SYN) channel handler, a control (D) channel handler with hardware CRC (Cyclic Redundancy Check) and parity generation and checking, an audio (B) channel handler, and timing recovery. Figure 2-7 is a block diagram of the formatter.

The formatter is enabled by programming MECTR1[3:2] to 11.

Figure 2-7 CT2 Formatter Block Diagram



2.3.1.2 Device Selection: CFP/CPP

The Am79C411 can operate as either a CFP (Cordless Fixed Part, or base station) or a CPP (Cordless Portable Part or handset). The operating mode is determined by the DEVMODE register. The mode can be changed only while the CT2 Formatter is held in clear mode by programming the RXMUX and TXMUX registers for clear.

2.3.1.3 UKF1 Authentication

UKF1 Authentication is a proprietary security arrangement requiring special licensing available through the CT2 Founders Group. Details of approved authentication circuitry embedded in the PhoX device are available from the Secretariat of the CT2 Founders Group.

2.3.1.4 Multiplex Selection and Formatter Clear

ETSI document I-ETS 300 131 defines four different burst structures: MUX1.2, MUX1.4, MUX2, and MUX3. In this document, the term MUX1 refers to either MUX1.2 or MUX1.4. The multiplex mode for the transmitter is programmed in the TXMUX register, and the mode for the receiver is programmed in RXMUX. Software selects the appropriate multiplex depending on the device mode and call status. In order to accommodate protocol requirements, the receive and transmit multiplex modes are independent; for example, it is possible to transmit packets in MUX2 and receive packets in MUX1.2.

The CT2 Formatter is in clear mode when both RXMUX and TXMUX are programmed to 03 hex. Clearing the formatter resets the state machines in the formatter but does not return user accessible registers to their default values.

When the CPP transmits in MUX3 mode, its receiver should be programmed to receive MUX2. When the CFP is receiving in MUX3 mode, its transmitter should be programmed for MUX2 mode, and transmission should not be allowed to start until the appropriate protocol is received from the CPP.

Hardware disallows transmission of MUX1 until RXTMGR[7] indicates that the receiver is synchronized.

Software Notes:

- 1. When changing the transmit multiplex, program TXMUX while the transmit buffer is empty.
- 2. When the CFP switches from MUX3 to MUX2, it must release its synchronization to the CPP by writing to SYNCTR.
- 3. For optimal performance, the formatter should be enabled or disabled in MECTR1[3:2] only when RXMUX and TXMUX are programmed for clear mode. It is recommended that all formatter registers be configured before exiting clear mode. Clear MECTR1[3:2] before putting the device in shutdown mode.

2.3.1.5 Starting and Stopping Transmission

To initiate transmission, the transmit buffer must be filled with a code word and TXDISAB[1:0] must be cleared. If the transmitting device is a timing slave, that is, a CPP in MUX1 or MUX2 or a CFP in MUX3, then it must also have synchronized its receiver by having detected a SYN channel pattern. The synchronization status can be read in the RXTMGR register.

Transmission stops at the end of the frame carrying the last bit of the current code word, including CRC and parity bits after TXDISAB[0] is set. TXDISAB[1] aborts transmission immediately at the end of the current frame. The CPP MUX3 transmission stops automatically immediately after reception of a valid SYNCF marker from the CFP.

2.3.1.6 500-Hz Burst Synchronization Port

The Am79C411 can be synchronized to an external 500-Hz signal in slave mode to meet the requirements of I-ETS 300 131 Annex N for CFPs. Burst synchronization control is programmed in the BSYNC register. The feature does not apply to the CPP. To enable pin P1.6 to function as the SYNC input pin, program P1SRC2[6].

As a slave, the PhoX controller phase-locks to the incoming 500-Hz SYNC signal on pin P1.6. An initial acquisition circuit aligns the internal timing with the first 500-Hz pulse at the P1.6 pin to assure rapid locking. Transmission and reception is inhibited until this alignment is achieved.

Input drift in excess of the tracking limit results in the PLL pulling to that tracking limit. Actual input drift must remain below the CT2-imposed 50-ppm (absolute) limit for system compliance. The device supports larger peak jitter input, as long as the long term drift specifications are observed. PLL adjustments are made in 108-ns increments at 125- μ s intervals until either the phase discrepancy is compensated or the tracking limit is reached.

CFP transmission of bit B1 in MUX1 starts at the antenna nominally 7 bit periods after the SYNC signal rises. Software programs the receive timing, indirectly adjusting the transmit data timing to meet the 7-bit delay requirement. The programmable delay in conjunction with the programmed modem delay register allows any total RF delay (transmit + receive) up to 6.9375 bits (96 μ s). Figure 2-8 depicts burst synchronization in MUX1.2. For MUX1.4, B channel timing relative to SYNC is identical. The burst timing of MUX2 is the same as that of MUX1.2.

Software has visibility of the SYNC input signal on the P1.6 pin to time various software tasks. Just as P1.6 can generate interrupts, the SYNC signal can be programmed in register bits P1TRIG[6] and P1MASK[6] to generate interrupts on either the rising or falling edge, which is useful for counting frames for intermittent transmissions like the CT2Plus standard MUX4 format.

Programming Sequences:

The BSYNC register must be programmed before the CT2 Formatter and the B Channel Multiplexer are enabled in MECTR1[4:2], and MECTR1[4] (B Channel Multiplexer and frame clock enable) must be set for the CT2 Formatter to function correctly in synchronized mode.

1.	Configure synchronization mode.	BSYNC[7:6] = 11 P1SRC2[6] = 1
2.	Enable the SYNC phase-locked loop.	MECTR1[4] = 1
3.	Enable the CT2 Formatter.	MECTR1[3:2] = 11

- 4. Initialize the CT2 Formatter registers.
- 5. Release the CT2 Formatter from clear mode.

a.	If CFP is initiating the call	TXMUX[1:0] = 10 RXMUX[1:0] = 10
	transmissions will be synchronized to the SYNC signal.	
b.	If the CFP is receiving a MUX3 message initiated by the CPP	RXMUX[1:0] = 11 TXMUX[1:0] = 10
	the CT2 Formatter automatically decouples ra- dio timing from the 500-Hz SYNC timing in order to recover the MUX3 message. After a suitable MUX3 message is received, change to receive MUX2.	RXMUX[1:0] = 10
	This automatically couples the CFP radio timing to the 500-Hz SYNC timing.	





2.3.1.7 Timing Recovery

The CFP is generally the timing master, deriving its bit-rate timing from the 18.432-MHz crystal or clock source connected to the PhoX chip. Even as a timing master, the CFP's data recovery circuit is capable of extracting and tracking receive data bit timing in order to locate the data sampling window, but this tracking does not affect RF control signals or transmission time.

The CPP is a timing slave to the CFP in multiplex modes MUX1 and MUX2, deriving its reference timing from the receive data bit stream. This extracted timing is then used to set the transmitter timing. Adjustments to the timing are made only during the receive portion of the frame and are based on receive data transitions.

MUX3 is the exception condition that reverses the master and slave roles of the CFP and CPP, such that the CPP is the timing master and the CFP is the timing slave. In this case, the CFP tracks the data rate of the received CPP transmission in order to completely recover the entire MUX3 data sequence.

The RXTMGR register controls timing recovery functions.

A dual-speed, digital phase-locked loop recovers the receive clock based on data level transitions. High speed (651 ns/bit adjustment max) is used for quick timing acquisition; for example, at the beginning of a MUX3 reception, and low speed (108 ns/bit max) is used to maintain phase lock once the timing reference has been established. The acquisition speed function is largely automatic, although speed can be forced to the slow mode by programming RXTMGR[1]. The speed automatically switches to low speed when the receiver detects a SYN channel marker, as reflected in RXTMGR[6].

Receive data is sampled either once, at the mid-point of the predicted bit interval, or three times, separated by 1.7 μ s centered at the mid-point of the predicted bit interval, under control of RXTMGR[2].

RXTMGR[0] is called Receive Timing Recovery Enable. It enables two functions in the CPP:

a. Adjustment of data sampling according to receive data edges.

Under normal conditions, the PLL attempts to locate the sampling instant 6.9 μ s after the previous valid data boundary. This function allows the PhoX device to move the sampling point for robust reception as the data position fluctuates with variations in radio conditions and receiver slicer-level tracking.

b. Adjustment of receiver radio timing and transmitter timing.

The receiver radio control signals as well as the subsequent transmission timing will be affected by the adjustments made by the phase-locked loop attempting to track the receive data.

The control bit must be set to allow the CPP to track the CFP timing in MUX1 and MUX2.

In the CFP, Receive Timing Recovery Enable functions differently. The radio control timing (transmit and receive) and the data transmission timing are unaffected by the phase-locked loop, regardless of the state of Receive Timing Recovery Enable. If the bit is cleared, data sampling is fixed and will be located at the middle of the adjusted ideal bit timing. The adjusted ideal bit timing is defined to be the ideal timing at the antenna as described by the CAI, modified by the programmed modem delay. For the CFP case, setting Receive Timing Recovery Enable enables adjustment of data sampling, as described above for the CPP. In general, allowing this sampling time adjustment increases CFP tolerance to receive drift and jitter.

MUX3 is an exception for both the CFP and the CPP. Receive Timing Recovery Enable must be enabled in both CFP and CPP in order to best recover the MUX3 frame. The CFP will actually track the receive data timing. The CPP will not track the CFP timing, but it will adjust its receive sampling location to the middle of the actual recovered bit.

Although the CFP is the radio link timing master, except in MUX3, it can be slaved in turn to the 500-Hz SYNC signal, effectively making the SYNC source the link timing master.

2.3.1.8 SYN Channel Operation and Link Synchronization

The synchronization (SYN) channel is present in multiplexes MUX2 and MUX3 in order to gain burst synchronism. In MUX2, the SYN channel is a 10-bit preamble and a 24-bit Channel Marker (CHM) or Synchronization Pattern (SYNC). In MUX3, it is a 12-bit preamble and a CHMP (CHM for a CPP) pattern. The RXMUX and TXMUX registers control the CHM/SYNC selection for the receiver and transmitter respectively. The polarity of the CHM or SYNC (i.e., CFP or CPP) is determined by the DEVMODE register.

The receiver searches the incoming data stream for either a CHM or a SYNC pattern and reports the synchronization status in the RXTMGR register. Once a CHM or SYNC pattern is received, a CHM/SYNC interrupt is propagated to the central interrupt controller. The cause of the CHM/SYNC interrupt is reported in the CMSSRC register. Individual bits in CMSSRC are enabled in the CMSMASK register. Once the CHM or SYNC pattern is located, the receiver frame timing remains locked. If the receiver fails to receive any subsequent CHM or SYNC patterns, it generates a CHM/SYNC interrupt, which is reported as a SYNC error in CMSSRC[3], subject to masking in CMSMASK[3].

Writing the SYNCTR command releases the receiver to resynchronize by seeking the next CHM or SYNC pattern. SYNCTR must be written to initiate reception and to re-establish link timing; for example, when a CFP completes MUX3 reception and starts MUX2 transmission. Since the transmitter timing is linked to the receiver, transmissions are also stopped on a SYNCTR command.

Ordinarily, the SYN channel must be received entirely without error to cause frame timing to lock or to avoid error interrupts after frame timing is already locked. The error tolerance feature offers the option of recognizing the SYN pattern with up to one error in any bit location. It is enabled in RXMUX[3] and may be used dynamically to lock the timing to even a corrupted SYN channel and then to report any bit errors that occur after lock by switching error tolerance off. Applications include robust reception of intermittent transmissions, such as CT2Plus MUX4.

2.3.1.9 D Channel Operation

The D channel exists in all multiplexes for link management. Layer three messages consist of a number of packets, each made up of one to six code words. Code words are eight octets long. Each code word includes six data octets, followed by 15 CRC bits and one parity bit such that the whole 64-bit code word has even parity. The first code word of each packet is preceded with a D Channel Synchronization (SYNCD) pattern. Between packets, either a predefined FILL-IN packet or an IDLE_D pattern (alternating ones and zeroes) is transmitted to fill unused D channel bandwidth.

Hardware handles SYNCD, IDLE_D, CRC, and Parity insertion and checking. Generation and interpretation of the data octets is left to software.

The Am79C411 has double buffers capable of retaining two entire code words. Selection between single and double buffering is made in DEVMODE[6], which must be programmed while the formatter is in the clear mode (see Section 2.3.1.4).

Figure 2-9 summarizes how the PhoX IC operates the D channel.

Figure 2-9 Operation of the D Channel

Transmitter	D CHANNEL	Receiver
		—— Software starts frame sync acquisition using SYNCTR command.
		—— Software writes RDATAC register to start hardware SYNCD search.
Software sets a bit in the SYNCDC register to insert the SYNCD pattern	←	Hardware recognizes SYN Channel. \rightarrow CHM/SYN interrupt
(Performed automatically if	SYNCD	Hardware recognizes SYNCD.
	Octet 1	\rightarrow SYNCD interrupt
Software loads the Transmit Buffer	Octet 2	Hardware checks header for last code word in packet
	Octet 3	
	Octet 4	
	Octet 5	Receive Buffer full \rightarrow DRXFULL (or DRX HALF FULL) interrupt.
Buffer empty \rightarrow DTXEMPTY interrupt	Octet 6	Software reads the Receive Buffer (RXBUF0–5).
CRC and parity inserted by hardware. End of code word \rightarrow DTXEMPTY interrupt	CRC	CRC/Parity checked by hardware.
(or DTX HALF EMPTY)	Parity CRC	$\frac{1}{1}$ CRC/Parity Error \rightarrow DRXERR interrupt
Software may reload the buffer with data code words for variable length packets or start again for address code words or for FILL-IN.	•	If last code word in packet, hardware issues RDATAC to seek next SYNCD if enabled in DEVMODE[6]. Otherwise, RDATAC must be issued from software.
Hardware inserts IDLE_D when there are no more code words.	IDLE_D IDLE_D	Hardware continues to store data (data code words) until RDATAC is issued by hardware or software.





Figure 2-11 D Channel Transmit Timing Constraints, MUX2, Double Buffering



2.3.1.9.1 D Channel Transmit Operation

When a packet is to be transmitted, software loads the transmit buffer with the six data octets of the code word. If the actual content of the code word is less than six bytes, all six bytes need not be written, but TXBUF5 must always be written in order to trigger the hardware response. Transmission is enabled by programming the TXDISAB register. The transmitter drives the data octets, preceded by the SYNCD pattern as necessary and followed by the automatically generated CRC field and the parity bit. When in MUX2, hardware always locates the SYNCD pattern in the last 16 D channel bits of the MUX2 frame.

The transmitter functions in single- or double-buffer mode. Double-buffer mode is available to increase the real time available for processing code words, especially in MUX2.

In single-buffer mode, software must control the insertion of SYNCD by programming SYNCDC before the code word is written to the buffer. When the buffer empties,

the formatter propagates a DTXEMPTY interrupt to the central interrupt controller through the MISRC0 register, subject to masking in MIMSK0, indicating available buffer space for an additional code word. DTXEMPTY status is reported in the DCHSTAT register and occurs either when hardware reads the last transmit buffer byte or when the end of the code word (parity bit) is transmitted, depending on how DTXCTR[1] is programmed. Software must respond to DTXEMPTY within approximately 1 ms in MUX2 if the buffer requires reloading, which is the case with a data code word directly following an address code word, as shown in Figure 2-10.

The transmit buffer may be loaded with up to two complete code words if double buffering is selected in DEVMODE[6], relieving the 1-ms processing speed requirement just mentioned and allowing instead approximately 7-ms in MUX2, as shown in Figure 2-11. When double buffering is enabled, automatic SYNCD insertion is also enabled, effectively obsoleting the SYNCDC register by automatically inserting SYNCD only before all legal address code words. In double buffer mode, interrupts are generated when the buffer is empty and half-empty, indicating buffer space for either one or two code words. In the figure, the empty indicator at the right is shown in parentheses to demonstrate that it occurs only if software fails to write a new code word after the half-empty interrupt.

Software must observe the following programming order when using the double buffers:

- 1. Establish double buffer mode in DEVMODE[6] before enabling the formatter.
- 2. Recognize Transmit Buffer Empty or Half-Empty Interrupt, if applicable.
- 3. Program DTXCTR, if a change is necessary.
- 4. Load the buffer, TXBUF0–TXBUF5.
- 5. Program TXDISAB, if necessary, to start or stop transmission.

After the first code word of a packet is sent, the transmitter continues transmission in one of three ways:

- 1. If the buffer has not been loaded with a new code word, the transmitter sends IDLE_D after the check field and parity bit.
- 2. If a new data code word is loaded in the buffer, the transmitter begins sending the new code word, prefixed with SYNCD in the case of address code words, in the next bit position after the check field and parity bit.
- If continuous transmission is enabled in DTXCTR[0], the six octets will be repeated in successive fixed length packets, separated by 48 IDLE_D bits. The DTXEMPTY interrupt is not asserted in this mode.

FILL-IN

Continuous transmission mode is intended for transmission of the predefined fixed-length FILL-IN code word in MUX2. The FILL-IN octets must be written to the buffer in the same manner as any other code word. Once DTXCTR[0] is set, the code word will repeat indefinitely until DTXCTR[0] is cleared. Each transmitted packet is prefixed with SYNCD and separated by 48 bits of the IDLE_D pattern. In MUX1, continuous transmission mode will violate the minimum code word transmission rate due to the automatic insertion of 48 IDLE_D bits, so FILL-IN must be written anew to the buffer for each transmitted packet.

IDLE_D

When the transmit buffer empties and the last parity bit is transmitted, the transmitter automatically generates the IDLE_D pattern output (alternating 1 and 0). In MUX2, each new packet marked with SYNCD is automatically preceded by 16 IDLE_D bits in the first 16 D channel bits of the transmit frame containing SYNCD. Forty-eight IDLE_D bits are also automatically inserted between packets during continuous transmission of the same fixed-length packet.

2.3.1.9.2 D Channel Receive Operation

Receiver D channel synchronization cannot be locked until frame timing has been established with the SYN channel. The PhoX device acquires D channel packet synchronization by seeking the SYNCD pattern at the beginning of each new packet when an RDATAC command is issued. The SYNCD pattern is 1100.0100.1101.0111, in chronological order. After recognizing a SYNCD pattern, the D channel receiver drives a CHM/SYNC interrupt to the interrupt controller and starts collecting the following six bytes of D channel data, which are the code-word octets. The cause of the interrupt is reported as SYNCD in CMSSRC[2] and is subject to masking in CMSMASK[2].

The six D channel octets are loaded in the receive buffer. The following 16 bits of CRC and parity are routed to a CRC/Parity check circuit, which generates a DRXERR interrupt in case of error. At the end of the check field reception, the DRXFULL interrupt notifies software that the receive buffer contains a code word. The check field is not loaded in the receive buffer. DRXERR and DRXFULL interrupts are reported in the DCHSTAT register and are forwarded to the MISRC0 register in the interrupt controller, masked by MIMSK0.

Two tasks must be completed at the end of each code word: (1) the code word must be read from the buffer and (2) the decision to resynchronize the D channel must be made. If the buffer is not read by the time the beginning of next code word arrives, the new code word will be lost and an overflow interrupt will occur in the CRC/Parity Error indicator. Enabling the double buffers increases the real processing time available for the higher layer software of the receiver, extending the maximum processing time from 1 ms to approximately 7 ms in MUX2. Double buffers are enabled in DEVMODE[6].

The D channel must be resynchronized after every packet before a new packet can be received, but it must not be resynchronized between code words within a variable length packet. The decision to resynchronize the D channel can be done in either hardware or software. Hardware determines whether the code word just received is the last of the current packet, as defined by the FT and endwrd bits of the first octet. When the DEVMODE[6] is set, hardware will automatically issue an RDATAC command to begin a new search for SYNCD if the code word just received was the last of its packet and was received without CRC, parity, or overflow error. Error conditions require software intervention using the RDATAC command to clear D channel synchronization. The D channel synchronization clear function can be controlled completely by software by clearing DEVMODE[6] and using the RDATAC command. If this function is performed in software, the decision to issue RDATAC must be evaluated before reception of the next code word begins.

Note: Software always has responsibility for issuing the first RDATAC to initiate D channel reception.

2.3.1.10 B Channel Operation

The B channel handler aligns the 64 B channel ADPCM audio bits within the MUX1 transmit and receive frames and scrambles the data to ensure random output data sequences for timing recovery and spectral considerations. In the transmitter, bits 3, 4, 6, 9, 14, 16, 18, 19, 20, 22, 23, 27, 28, 29, 30, 31, 34, 35, 37, 40, 45, 47, 49, 50, 51, 53, 54, 58, 59, 60, 61, and 62 are inverted (scrambled). In the receiver, they are reinverted (descrambled).

The B channel is inhibited until RXTMGR[7] indicates that the receiver is synchronized. The B channel may be enabled by programming the BVALID register, allowing data flow between the common air interface in MUX1 and the PhoX chip audio circuits. Before BVALID is asserted, transmit B channel data is forced to zero. The 8-kHz frame clock must be enabled in MECTR1[4] for a minimum of 1.25 ms before asserting BVALID. It is recommended that the B channel source and destination (i.e., transcoder, B channel port or encryption port) be initialized before setting BVALID.

To meet CT2 handset delay requirements, the total round-trip B channel delay, including A/D conversion, CT2 link transmission, CT2 link reception, and D/A conversion, is approximately 1.94 msec.

The 8-kHz ADPCM frame synchronization clock, which may appear on the BDP2_OUT4 multifunction pin as the CLK8K signal, tracks the CT2 recovered timing and may jitter by as much as ± 108 ns per 125- μ s frame when formatter receive timing recovery is enabled in a CPP.

2.3.1.11 RF Delay Compensation

The modem delay measurement facility provides a means for compensating RF delay to meet CT2 specifications for relative timing of receive and transmit portions of the frame at the antenna. The facility includes a measurement tool and a control tool. The measurement tool is useful but not necessary, and it requires the telephone RF circuitry to provide a radio frequency loopback at the antenna from transmitter to receiver. Measurement can also be done in the laboratory and the results can be applied with the control tool, which is simply a programmed delay field in the MODDLY register.

The CAI specifies a fixed timing relationship between receive and transmit subframes in Figure 5.1 of I-ETS 300 131, measured at the antenna. The following equation represents that relationship:

 $t_{CFPRX \rightarrow CFPTX} = t_{RXRF} + t_{ADJ} + t_{TXMOD} + t_{TXRF}$

where the left side of the equation is the time difference between the last received bit of one frame and the first transmitted bit of the next frame for the CFP, specifically 4.5 bit periods in MUX1.4 and 6.5 bits in MUX1.2 and MUX2. Receive data must pass through the receiver RF circuitry and demodulator, inducing delay t_{RXRF} . Likewise, transmit data experiences delay $t_{TXMOD} + t_{TXRF}$ in the modulator and the RF sections. The term t_{ADJ} is the adjustment made by PhoX device hardware to compensate the right-hand side of the equation and is applied to the transmit controller so that CT2 specifications are met. The measurement operation is initiated by a software command in the MODTMG register and would normally occur at power-up. During measurement, the transmitter and receiver are simultaneously enabled; that is, the TXEN and RXEN pins are both High, so that transmit data is looped back to the receiver via the antenna. The measurement circuit counts the delay between transmission and reception of CHM and returns the result, t_{MDM} , in the MODDLY register.

 $t_{MDM} = t_{TXMOD} + t_{TXRF} + t_{RXRF}$

 $t_{CFPRX \rightarrow CFPTX} = t_{MDM} + t_{ADJ}$

MODTMG[1] controls whether the measured delay t_{MDM} is used by the frame formatter and normally should remain cleared. If MODTMG[1] is set, t_{ADJ} works as if t_{MDM} is zero.

To measure delay, the following sequence should be followed:

- 1. Initialize the transmitter mode: TXMUX=02 for CFP, TXMUX=03 for CPP.
- 2. Initialize the receiver mode: RXMUX=02 for CFP and for CPP.
- 3. Load the D channel transmit buffer, TXBUF.
- 4. Set the MEASURE DELAY bit in the MODTMG register: MODTMG=01.
- 5. Enable receive timing recovery: RXTMGR=01.
- 6. Enable transmission by clearing TXDISAB[1:0].
- 7. Poll the MEASURE DELAY bit, MODTMG[0], until it is cleared by hardware, indicating completion of the measurement. If the delay exceeds 6.9375 bits (96 μs), the measurement will fail and hardware will not clear the MEASURE DELAY bit, indicating an RF error. This requires a software timeout.

The measured delay in MODDLY may be moved to non-volatile memory, such as EE-PROM, for use in future link initiation sequences. To force the modern delay compensation to any arbitrary value or to a previously determined value, software writes the value to MODDLY and clears MODTMG[1].

2.3.1.12 Radio Interface

Figure 2-12 shows the basic radio interface signals.

Figure 2-12 Programmable Timing of RF Interface Controls



Table 2-5 Radio Interface Signals

Name	Signal	Description
Transmit Window	CT2TXEN	Provided for utility in testing and development, the CT2TXEN signal appears on the BDP2_OUT4 pin when appropriately programmed in BDMUX[6:5]. CT2TXEN is High while transmit data CT2TXD is active.
Transmit Data	CT2TXD, TXI/TXQ	Transmit data appears in either NRZ (pseudo-digital) or analog I/Q form at the TXI and TXQ pins, described in Section 2.3.3, CT2 Baseband Output Driver.
		It can also appear in true digital form as the CT2TXD signal on the BDP1_OUT3 pin when that pin is appropriately configured in the BD-MUX register. In this case it is also accompanied by a 72-kHz clock CT2TXCLK on pin BDP0_OUT2 (not shown), which rises at the beginning of each new bit.
		Analog I/Q data lags its digital equivalent by approximately 15.1 $\mu s.$
Transmit Enable	TXEN	The programmability of the rising edge of TXEN with respect to unfiltered digital transmit data is 868 ns \leq t _{TTD} \leq 32.1 µs in 3.47-µs increments, programmed in TDELAY[7:4].
		The programmability range of the falling edge of TXEN with respect to transmit data is $4.3 \mu s \le t_{TTL} \le 46 \mu s$ in $3.47 \cdot \mu s$ increments, programmed in TDELAY[3:0].
Receive Data	CT2RX	The CT2RX pin is the digital receive data input. The input is assumed to have been acted upon by an external FM discriminator followed by a slicer circuit to determine digital bit boundaries from the down-converted analog baseband signal by comparison to a varying reference voltage. The external slicer should include some amount of hysteresis for noise reduction and the CT2RX signal should have a rise time on the order of 1 μ s or less for optimal timing recovery response. Input to the slicer should be band-limited so that noisy radio conditions do not create numerous data transitions during the receive window because this may also negatively impact timing recovery.
		The pulse widths of data presented to the PhoX chip on the CT2RX pin influence timing recovery and will be affected by the external data slicer circuit. As the slicer level adjusts to balance the relative pulse widths of binary 1s and 0s, the nominal 13.88- μ s pulse width will vary. To guarantee initial recognition of the first SYN channel pattern presented to the pin, the pulse widths of data bits input to the CT2RX pin during the SYN channel must be within the range 13.88 ± 1.735 μ s. In the absence of significant jitter, pulse widths as low as 7.3 μ s will be accommodated, but synchronization will take longer on average, degrading proportionally to the slicer imbalance.
		Once synchronization is achieved, tolerance to pulse width variation improves. In the absence of jitter, pulse widths as low as 7.3μ s will be tolerated without error or loss of synchronization. Jitter will naturally degrade this performance, with tolerance being reduced proportional to the severity of the jitter.
Receive Enable	RXEN	The programmable delay from the end of digital transmit data to RXEN High is 11.3 μ s \leq t _{TRH} \leq 87.6 μ s with 3.47- μ s resolution, programmed in RDELAY[4:0]. RXEN always falls t _{RRL} = 6.9 μ s after the last data bit is received. RXEN can also be forced High regardless of the activity state of the CT2 Formatter to enable the radio receiver for scanning, programmed in RDELAY[5].

Name	Signal	Description
Slicer Control	SHCTR	The sample/hold control (SHCTR) pin provides timing for an external sample/hold circuit, which may be used to control DC offset in the receiver slicer.
Transmit Power Control	TXPWR*	The TXPWR pin is a control output synchronized to CT2 frame timing and controlled by software through the TPOWER register to accommo- date CT2 specifications for normal and low-power transmissions. De- pending on RF timing, TXPWR could be used alternatively for antenna diversity control.
Antenna Switch	ANTSW	Additionally, there is an output control called an Antenna Switch (ANTSW), intended to switch the antenna between the receive and transmitfunctions. ANTSW always goes High $t_{SWT}\cong 6.9\mu s$ before TXEN rises and goes Low when RXEN goes High. The ANTSW signal is multiplexed on the XINT2_ANTSW pin and is enabled for the ANTSW function under software control by programming RDELAY[6].
Clock	CLK4M*	TPOWER[0] enables a 4.608-MHz clock on the CLK4M pin and may be useful for external synchronous data processing or RF control circuits.

Table 2-5 Radio Interface Signals (continued)

Note:

*The signals are not shown in Figure 2-12.

2.3.2 RSSI

The receive signal strength indicator (RSSI) determines the value of the RSSI analog input pin, representing the level of the received RF signal. The circuit includes a 5-bit successive approximation A/D converter requiring approximately 10- μ s conversion time, during which the RSSI pin should be held constant within 1 LSB of resolution. The input is a high impedance, so the RSSI level may be developed across an external resistance driven by a current source.

The RSSI is enabled only when MECTR1[0] is programmed. The RSSI operates in synchronous and asynchronous modes, according to the CT2 link synchronization status reported in RXTMGR[7]. Asynchronous mode is intended for the channel scanning application and the A/D conversion begins immediately after a conversion request in the RSSISTAT register.

Synchronous mode is entered automatically when the link has synchronized. All conversion requests are synchronized to internal sampling pulses that occur only in the receive portion of the CT2 frame, as shown in Figure 2-13.

Setting RSSISTAT[7] requests a conversion and a valid result is returned in RSSISTAT[4:0] at the end of the conversion. Hardware signifies the end of the conversion by clearing RSSISTAT[7]. RSSISTAT[6] reports the level at port pin P1.7, allowing software to simultaneously assess the receive level and an external digital signal, for example, a free channel status signal.

Figure 2-13 RSSI Timing in Synchronous Mode



2.3.3 CT2 Baseband Output Driver

The CT2 baseband output driver drives data in one of two modes, I/Q or NRZ, defined by the control bit MODTEST[4]. There is also a test mode for RF development and test described in Section 2.5.2.

2.3.3.1 I/Q Mode

The default mode is I/Q. In this mode, the modulator is a baseband Gaussian-filtered minimum shift key (GMSK) modulator specifically designed to meet or exceed CT2 spectral requirements. Serial transmit data from the CT2 Formatter is digitally filtered and converted to two single-ended quadrature analog outputs, called TXI and TXQ. The outputs are intended to be externally mixed with the IF or RF carrier and summed to obtain the desired frequency modulated signal.

The Gaussian filter response is approximated as a 6th order Bessel filter with linear phase response and a 3-dB cut-off frequency of 57.6 kHz (i.e., the normalized 3-dB bandwidth $B_bT=0.8$). The D/A conversion samples at 4.608 MHz with 7-bit precision over a ± 0.5 -V AC range, DC referenced to the MREF pin. Net delay through the modulator, from digital input to analog output, is approximately 15.1 μ s.

The mathematical description of TXI and TXQ, depicted in Figure 2-14, is:

 $\begin{aligned} \mathsf{TXI} &= 0.5\mathsf{V}\cdot\mathsf{I}(t) + \mathsf{MREF} \\ \mathsf{TXQ} &= 0.5\mathsf{V}\cdot\mathsf{Q}(t) + \mathsf{MREF} \\ \mathsf{I}(t) &= \sin\left(\int \omega_{\mathsf{m}}(t) \mathsf{d}t \right) \\ \mathsf{Q}(t) &= \cos\left(\int \omega_{\mathsf{m}}(t) \mathsf{d}t \right) \end{aligned}$

where $\omega_{\rm m}(t)$ is the instantaneous GMSK message frequency, which has a range of ±18.0 kHz and the step response defined by the digital filter. Outputs are defined such that when I and Q are subjected to a quadrature mixer and a carrier $\omega_{\rm c}$, as in Figure 2-15, the result y(t) is:

 $y(t) = I \cdot \cos(\omega_c t) + Q \cdot \sin(\omega_c t) = \sin(\omega_c t + \int \omega_m(t) dt)$

The instantaneous frequency of y(t) is then $\omega_c + \omega_m(t)$ and there are no sidelobes. The frequency eye-diagram of y(t) is shown in Figure 2-16.

A passive single-pole low-pass filter with 3-dB frequency around 100 kHz is necessary at both TXI and TXQ outputs to remove sampling images at 4.608 MHz. The filter must have a minimum impedance of 1 k Ω . For stability, the maximum capacitance from pin to ground cannot exceed 100 pF.

To reduce frequency spread, the modulator ramps up smoothly when transmit data is driven to it from the CT2 Formatter. During the ramp-up period, I is zero and Q rises from zero to full scale so that the amplitude of y(t) increases smoothly from zero to full scale. Likewise, the modulator ramps down smoothly at the end of the transmission. Note that there remain two points of inflection at the beginning and ending points of the envelope of y(t) that require external smoothing.

The modulator must be enabled in MECTR1[5] to function and responds to the transmit data without software intervention. The MODTST register provides test modes, enabling the modulator to send fixed or externally generated data patterns for RF circuit evaluation.

Figure 2-14 Modulator Waveforms



Figure 2-15 Modulator I/Q Mixer Block Diagram



Figure 2-16 Modulator Eye Diagram for Three-Term Data Sequences



2.3.3.2 NRZ Mode

NRZ (Non-Return to Zero) mode creates a pseudo-digital waveform and is enabled by setting MODTST[4]. The output appears at the TXI and TXQ pins as a square wave of ± 0.5 -V amplitude biased around Vcc/2, as shown in Figure 2-17.





2.3.4 Fade Management

The PhoX controller offers many indicators allowing development of proprietary software algorithms to handle signal fades and interference conditions. These conditions can result in bit errors and even the loss of synchronization. Link quality indicators include the RSSI level, the D channel CRC and parity check, the SYN channel error check, the jitter indicator, and the B channel noise indicator. All of these factors should be considered in developing a comprehensive link maintenance algorithm. With the exception of the RSSI level, all indicators are available as interrupts.

2.3.4.1 Handling the Link

After software determines that a signal fade or interference condition exists, it may elect to program the CFP PLL timing recovery enable bit RXTMGR[0] to disable timing recovery. Disabling the timing recovery forces receive data sampling instants to occur at known locations relative to the CFP's own transmission timing. Radio control timing is unaffected. All of the link quality indicators remain operational so that they can be used to determine when the fade ends.

At the physical layer, the receive data input (CT2RX) pin should be preconditioned to minimize the number of erroneous data-level transitions that may occur within one 13.88- μ s bit period under noisy conditions.

2.3.4.2 B Channel Noise Suppression

Bit errors or poor link quality adversely affect voice channel performance and in some cases can result in extremely loud noise bursts at the earpiece. Noise suppression is an automatic feature enabled in DSPCTR[7] that immediately mutes the transcoder receiver under noisy conditions. Mutes may also be performed under software control.

B channel noise is detected in two ways:

- 1. Non-speech B channel content, indicating bit errors
- 2. Jitter in the CT2 common air interface received data, indicating poor reception quality or likely loss of link synchronization
- Automatic Noise Suppression: The NSCTR register, bits[3:2], selects whether the noise suppression algorithm responds to bit errors or jitter. NSCTR[1:0] defines how the algorithm responds to noise indicators, as shown in Figure 2-18. The bits control the number and size of the attenuation steps applied to the receive data in the muting sequence. Noise generally arrives in bursts, so the four columns of Figure 2-18 show the response of the noise suppression algorithm to multiple consecutive noise events (triggers) as a function of the mute sequence, NSCTR[1:0]. Each new trigger causes increased muting until the maximum muting for a given programmed mute sequence is reached. The MUTE register controls the length of each attenuation step during the recovery. At each new trigger, the mute length counter is restarted, and if the counter reaches its programmed endpoint, one attenuation step is removed. Figure 2-18 assumes that the noise triggers occur near the beginning of the sequence, and that none occur during the recovery phase. If a trigger does occur during the recovery phase, muting again increases one step per event until the maximum muting is reached and the mute length counter is restarted.
- Software-Controlled Noise Suppression: Jitter and B channel noise trigger information is available in interrupt form to the processor, allowing proprietary noise suppression software algorithms by applying a loss at RXATTN in the transcoder. Both interrupts appear in MISRC0[5] with corresponding status bits in NSCTR[7:6].

	1 trigger	2 triggers	3 triggers	4 triggers or more
Mute sequence 0 dB 0 dB -6 dB -6 dB -6 dB -6 dB -12 dB -12 dB -12 dB -12 dB -18 dB -18 dB Full Mute Full Full Full Full Full Full Full Full		0 dB -6 dB -12 dB -18 dB Full Mute	0 dB -6 dB -12 dB -18 dB Full Mute	
Mute sequence =01	0 dB _6 dB _12 dB _18 dB Full Mute	0 dB -6 dB -12 dB -18 dB Full Mute	0 dB -6 dB -12 dB -18 dB Full Mute	0 dB -6 dB -12 dB -18 dB Full Mute
Mute sequence =10	0 dB _6 dB _12 dB _18 dB Full Mute	0 dB -6 dB -12 dB -18 dB Full Mute	0 dB -6 dB -12 dB -18 dB Full Mute	0 dB
Mute sequence =11	0 dB -6 dB -12 dB -18 dB Full Mute			

Figure 2-18 Noise Suppression Muting Sequence

Noise Suppression Triggers: Noise due to bit errors results in B channel waveforms outside normal human speech patterns. This type of noise is given the name DSP noise because it is detected by analyzing the contents of the B channel in the codec digital signal processor. The noise detector calculates the ratio of the predicted received signal to the difference between the predicted and actual received signals and generates a muting trigger when the ratio falls below the threshold programmed in the NSTHR register. Therefore, increasing NSTHR causes the trigger to be more sensitive to noise and more apt to falsely trigger on genuine non-noisy speech. Lowering it causes it to be more tolerant.

B channel noise triggers are reported in NSCTR[6], enabled by NSCTR[5], and cause an interrupt, shared with the jitter interrupt, in MISCR0[5].

The JITCTR register defines an integrating mechanism to count jitter occurrences on the CT2 receive data pin CT2RX and generate noise suppression triggers. The jitter phase threshold field of JITCTR sets the width of a window centered on the bit boundaries of the ideal bit timing. If level transitions on CT2RX occur outside of this window, the jitter event count is incremented. The jitter event count is zeroed at the beginning of each new frame. The jitter event threshold field determines how many jitter events must occur within one CT2 frame period to merit a noise suppression muting response.

Jitter-based triggers cause the jitter interrupt (MISRC0[5], MIMSK0[5]) and are reported in NSCTR[7], so that software may respond to excessive jitter that could occur when a link fails.

2.4 AUDIO FUNCTIONS

2.4.1 Am79C411 ADPCM Transcoder

The Am79C411 provides an ADPCM transcoder, shown in Figure 2-19, capable of translating 32-kbps ADPCM data to 8-bit μ -law or A-law compressed PCM. The architecture allows a fully compliant CCITT G.721 ADPCM transcoder with gain control and DTMF injection for an all-digital system. (Due to the nature of the G.721 test sequences, bit-for-bit compliance to the test sequences is not possible with gains or added DTMF). The Am79C411 uses the CCITT-recommended tandem coding technique to minimize distortion due to multiple PCM \leftrightarrow ADPCM translations, such as those found in repeaters or digital PBX environments.

The serial PCM port pin definition is listed in Table 2-6. The pins have the default states shown until DSPCTR[2:0] is programmed to 100. (Note that the default value of DSPCTR is not a legal value.)

The Am79C411 acts only as a 500-Hz CT2 SYNC slave when using the serial PCM port.





Pin Name	Pin No.	DSPCTR[3:0] = 0000 (default)	DSPCTR[3:0] = x100 (A/µ PCM Voice I/O)
TE	62	High (weak pull-up)	Transmit PCM strobe input
RE	61	High (weak pull-up)	Receive PCM strobe input
PCMCLK	60	High (weak pull-up)	PCMCLK input
PCMOUT	59	High (weak pull-up)	Receive PCM output
PCMIN	58	High (weak pull-up)	Transmit PCM input

Table 2-6 Am79C411 PCM Port Pin Function Summary

The Am79C411 generates an internal 8-kHz frame clock phase-locked to the input 500-Hz CT2 frame clock, such that the rising edge of the internal 8 kHz corresponds to 500-Hz transitions, as shown in Figure 2-20. The 8-kHz clock, called CLK8K, will appear as an output at the BDP3_OUT5 pin if that pin is configured correctly in the BDMUX register, bits [6:5]. PCMCLK is the serial data clock input on pin 60 and may be 64, 128, 192, 256, 512, 1024, or 2048 kHz. Independent active-High input strobes TE and RE mark the transmit and receive time slots. TE and RE must be eight PCMCLK pulses wide, must be synchronized to the 8-kHz clock, and must not span the rising edge of the 8-kHz clock pulse. Transmission and reception are triggered by detection of the appropriate active strobe when the PCMCLK is High or going High.

Figure 2-20 Am79C411 A-law/µ-law PCM Port Timing



2.4.2 Dual-Tone Generator

The dual-tone generator is a feature for generating single-frequency (SF), dual-tone multi-frequency (DTMF), or alert tones. It requires the transcoder to be enabled in MECTR0[6] and supplied with frame clock in MECTR1[4]. Figure 2-21 is a block diagram of the dual-tone generator.

Each of the two tones has a programmable frequency and amplitude. Tone 1 frequency is programmed in T1FR1, T1FR2, and T1FR3, and its amplitude, relative to digital full scale, is programmed in T1AR. Likewise, tone 2 is defined by T2FR1, T2FR2, T2FR3, and T2AR. The two tones are summed to form the dual-tone signal. Care should be taken when programming amplitudes T1AR and T2AR to ensure that the summed signal does not overflow the digital full scale, resulting in clipping distortion. For example, if tone 1 has an amplitude of $-6 \text{ dB} (0.5 \times \text{full scale})$ and tone 2 has an amplitude of $-3 \text{ dB} (0.707 \times \text{full scale})$, the peak summed value is $1.207 \times \text{full scale}$, which will be clipped. Therefore, the amplitudes must be adjusted down to avoid distortion.

The tones are added to the transmit and receive paths of the codec, with independent gain adjustment in each path. Again, digital overflow should be avoided at the summing points by consideration of expected voice levels in the transmit and receive paths and the programmed transmit and receive tone levels. TTAR is the programmed loss applied to the summed dual-tone signal before it is added to the transmit audio data. RTAR is the loss applied to the summed dual-tone signal before it is added to the receive audio data.

Programming Notes:

- 1. All ten dual-tone generator registers must be initialized before the codec is enabled.
- 2. Writes to dual-tone generator registers are buffered so that it is possible to update all ten locations simultaneously. Dual-tone registers loaded by software are not advanced into the digital signal processor until the RTAR address is written. Therefore, any write to any dual-tone register must be accompanied by a write to RTAR, which must occur at the end of the register write sequence.

Figure 2-21 Dual-Tone Generator Block Diagram



2.4.3 B Channel Multiplexer and B Channel Port

The B channel multiplexer configures the B channel data paths, making connections between the transcoder, the CT2 Formatter, and the 32-kbps serial ADPCM ports. Figure 2-22 is a block diagram of the B channel multiplexer, which is configured by programming the BDMUX register. In order to function, the B channel MUX requires the 8-kHz frame clock to be enabled in MECTR1[4]. The six multifunction pins that make up the B channel port must be configured by programming BDMUX[7:5]. Figure 2-23 shows the timing of the B channel port. The 8-kHz frame clock will exhibit 108-ns jitter when the device is a timing slave to either the 500-Hz CT2 clock or to the CT2 radio link. The encryption port path may be used to scramble data for secure communication, and an application drawing is included in the hardware applications section of Chapter 5.

CT2 Formatter CT2 Transmit Data Selection BDMUX[3:2] <u>رون</u> to CT2 Common from CT2 Common 01 Air Interface Air Interface <u>10</u>0 Transmit Receive Loopback 3 FIFO FIFO 11 o ADPCM Codec ADPCM Receiver Data Selection BDMUX[1:0] 00 0 Loopback 1 01 <u>10</u>0 to ADPCM Decoder ADPCM from ADPCM Encoder ADPCM О Transmitter <u>i 11</u>0 Receiver B Channel Port **B** Channel Output Port Selection BDMUX[4] **B** Channel B Channel 0 BCHOUT Input Port Output Port BDP0_OUT2 BDP1_OUT3 **BCHIN** enabled by enabled by pin С pin BDMUX[6:5]=00 BDMUX[6:5]=00 Encryption Encryption RXENCOUT BDP5_OUT11 TXENCIN Input Port Output Port BDP4_OUT8 enabled by enabled by pin pin BDMUX[7]=0 BDMUX[7]=0 Frame clock BCLK BDP2 OUT4 Timing and bit clock pins pin enabled by configured by CLK8K MECTR1[4]=1 BDP3_OUT5 BDMUX[6:5]=00 pin

Figure 2-22 B Channel Multiplexer Diagram

Figure 2-23 B Channel ADPCM Port Timing



2.4.4 Biasing

The biases of analog blocks are determined by an internal bandgap reference. IREF is the current reference that must be tied to analog ground through a temperature stable 61.9-k Ω , 1% resistor. The IREF pin is high impedance when the device is in shutdown mode. Because of its high input impedance, the IREF pin may be susceptible to noise. Therefore, external components connected to the pin should be located as close as possible to the IC and away from noisy signal traces.

The CFILT pin filters the internal analog reference voltage. Two capacitors, $10-\mu$ F low-frequency capactor (e.g., electrolytic) in parallel with $0.1-\mu$ F high-frequency capacitor (e.g., ceramic), must be tied from the CFILT pin to analog ground. The bias network performs a 108-ms rapid charge acquisition procedure after reset to bring analog circuits to their approximate DC bias point, after which the CFILT pin provides a 5-Hz single-pole, low-pass filter for AC rejection that is not affected by the shutdown mode.

The internal references are automatically powered down when the PhoX device is in shutdown. Upon exit from shutdown, approximately 300-µs stabilization time is required.

MECTR0[5] is a control bit that disables the internal analog references for all analog circuits, including the RSSI and CT2 Baseband output (TXI and TXQ). The bit must be cleared in order to use any analog function. Setting MECTR0[5] powers down the internal references for minimal power consumption in shutdown mode or when no analog circuits are necessary. Upon exit from the disabled state, references require approximately 300 µs to stabilize.

2.5 DEVELOPMENT SUPPORT

2.5.1 Emulation Mode

Emulation mode is for code development using an 8051-family emulator and is entered by driving the TRI1 pin to ground while reset is active. Emulators provide the debug advantages of instruction stepping, breakpoints, visibility of internal microcontroller registers, and a convenient program download procedure. In Emulation mode, an external processor with 8051 bus timing, shown in Figure 2-24, drives the P0, P1, P2, P3, and ALE inputs of the PhoX IC, replacing the on-chip 8032.

The PhoX chip in Emulation mode behaves as in normal mode, except as follows:

- 1. All of the on-chip 8032 ports go to the high-impedance state, including PSEN, ALE, P0, P1, P2, and P3 buffers.
- 2. The CS0_INT0 pin takes the INT0 output function, which may be used to drive the INT0 (P3.2) input of the emulator. The CS0 function is not available.
- 3. The CS1_INT1 pin takes the INT1 output function, which may be used to drive the INT1 (P3.3) input of the emulator. The CS1 function is not available.
- 4. The CS2_CPUCLK pin takes the CPUCLK output function, which may be used to drive the clock input of the emulator. The CS2 function is not available.
- 5. The ALE pin takes the ALE input function, which must be used to time bus transactions on the P0 and P2 buses.
- 6. The watchdog timer is disabled and does not generate periodic resets.
- 7. The T0 and T1 (P3.4, P3.5) 18-kHz clock inputs are not available to the emulator.
- 8. The 256-byte RAM in 8032 internal data space is not available for use by the emulator.

Figure 2-24 Driving the Am79C411 with an 8051-Family In-Circuit Emulator



2.5.2 CT2 Test Facilities

The PhoX IC provides test ports for the CT2 Formatter and the modulator (transmit baseband driver) to ease system debug.

Modulator Test Mode

The modulator test mode allows RF development to proceed without functional CT2 software by driving the modulator with either fixed patterns or externally generated arbitrary data. It operates with either NRZ or I/Q output data type and requires MECTR1[5] to be set. Figure 2-25 demonstrates the data sources for the modulator. The MODTST register bit [2] configures the modulator for the test mode. MODTST[1:0] defines the data pattern to be modulated. The modulator provides three internally generated fixed patterns: all zeroes (i.e., $\omega_m(t) = -2\pi \cdot 18$ kHz), all ones ($+2\pi \cdot 18$ kHz), and alternating ones and zeroes ($\omega_m(t)$ varies over $\pm 2\pi \cdot 18$ kHz). In the externally generated test pattern mode, any arbitrary data pattern can be injected at the BDP1_OUT3 multifunction pin with data transitions timed by the rising edges of the 72-kHz clock output at the BDP0_OUT2 pin. In test mode, the modulator does not perform ramp-up or ramp-down sequences.To correctly configure the multifunction pin, BDMUX[6:5] must be programmed to 11 and MODTST[2] must be High.

Figure 2-25 Data Source Selection for Modulator Test Mode



CT2 Transmitter Digital Output: The CT2 Formatter transmit data output appears in digital form at the BDP1_OUT3 pin when the BDMUX[6:5]=11 and MODTST[2]=0. Data changes on the rising edge of a 72-kHz clock that appears on the BDP0_OUT2 pin. The transmit data strobe, CT2TXEN, appears on BDP2_OUT4 and is High during valid transmit data. The digital transmit data of one PhoX chip may be directly connected to the receive data of another, as shown in Figure 2-26, to eliminate the radio link during software development. The TXI pin, emitting transmit data in NRZ format, can be used rather than BDP1_OUT3 if the 1.0-Vpp pseudo-digital TXI output is externally modified to meet digital electrical specifications for V_{IH} and V_{IL}.

Figure 2-26 Eliminating the RF Front-End During Software Development



B Channel Injection/Monitoring: The B channel multiplexer and B channel port are useful tools for validating B channel continuity and bit error rate. Connections are shown in Figure 2-27. The BDMUX register controls B channel routing. Multifunction pins are configured for B channel ports by programming BDMUX[6:5]=00. 8-kHz frame boundaries are determined by the CLK8K output on the BDP3_OUT5 pin and 32-kHz bit timing is the BCLK output on the BDP2_OUT5 pin. Data may be injected into the B channel by driving the BDP1_OUT3 pin. Input B channel data on BDP1_OUT3 is clocked into the PhoX device on rising edges of BCLK. B channel input may also be driven on the encryption input function of the BDP5_OUT11 pin (not shown). B channel output received from the CT2 link is available in the BCHOUT signal on the BDP0_OUT2 pin and in the encryption signal on the BDP4_OUT8 pin (not shown).

Figure 2-27 B Channel Injection and Monitoring



D Channel and SYN Channel Injection/Monitoring: Normally, D channel transmit data is driven by the microcontroller through the transmit buffer. D channel injection, shown in Figure 2-28, allows an external circuit to drive the transmit D channel serially. The B channel port pins must be configured for the D channel function by programming BDMUX[6:5] to 10 and the DMONIT register, bit 1, must be programmed High to select injection. Input is sampled on rising edges of the transmit clock pulses, which appear on BDP3_OUT5. The correct number of clock pulses for a given multiplex occur during the D channel time slots. For example, in MUX1.4 two groups of two clock pulses occur per frame, corresponding to the beginning and the end of the transmit frame. Data is presented in the D channel of the common air interface in the order in which it is received. The external circuit is responsible for generating the IDLE_D and SYNCD patterns as necessary.

Setting DMONIT[0] enables SYN channel injection or monitoring. In this case, external circuitry is responsible for driving all data except for preambles, including CHM and SYNC patterns and the B channel. The clock output on BDP3_OUT5 drives pulses during each D, B, CHM, or SYNC time slot, but not during preamble time slots.

Clearing DMONIT[1] puts the D channel port in output (listen only) mode. In this case, transmit D channel activity, controlled by the microcontroller, may be monitored by an external circuit. The BDP1_OUT3 pin follows the D channel transmit data, and BDP3_OUT5 provides clocks. Data transitions are on falling clock edges. If DMONIT[0] is set, the output includes D and B channels and CHM and SYNC patterns.

The receiver has a listen-only output on the BDP0_OUT2 pin, driving either D channel data only (DMONIT[0]=0) or D and B channels and SYNC and CHM patterns (DMONIT[0]=1). The associated DRXCLK clock pulses are outputs of the BDP2_OUT4 pin. Data changes on falling clock edges.

Figure 2-28 D/SYN Channel Injection and Monitoring



2.5.3 B Channel Loopbacks

Figure 2-29 shows the various B (voice) channel loopbacks provided in the PhoX chip. These loopbacks can be used to measure analog performance and isolate distortion sources and are programmed in the BDMUX register. Loopback 3 allows a PhoX device to behave as a reference CFP for the handset round-trip delay measurement. When used as a reference CFP, the effective loopback delay is approximately 1.62 ms.

Figure 2-29 B Channel Loopbacks







3.1 MEMORY MAP

The user registers and RAM reside in the 64-kbyte external data space of the 8032, as shown in Table 3-1. The controller also has an internal data space that includes 256 bytes of RAM and special function registers, which are described in the microcontroller section of the data sheet. In Table 3-1, the following conventions apply:

* = register described out of numerical sequence

- x = default value of bit is unknown
- $\underline{x}, \underline{0}, \underline{1}$ = reserved or unused bit
- n/a = not applicable

	Register					
Data Space	Mnemonic	Address	Access	Default	Description	Page
CS1		0000-EFFF	r/w		ext RAM, not Emulation mode	2-6
CS0		F000–F3FF	r/w		ext I/O 1, not Emulation mode	2-6
CS2		F400–F7FF	r/w		ext I/O 2, not Emulation mode	2-6
Address	reserved	FF00–FF0E		XXXX XXXX		
Decoder	ADRDEC	FF0F	r/w	<u>0xxx xx01</u>	chip select control	3-4
	unused	FF10–FF1F				
Parallel	P1SRC0	FF20	r	<u>0000 00</u> 00	P1 interrupt source 0	3-5
Port	P1SRC1	FF21	r	<u>0000 00</u> 00	P1 interrupt source 1	3-5
	P1SRC2	FF22	r/w	<u>0</u> 0 <u>00</u> 0000	P1 interrupt source 2	3-6
	P1MASK	FF23	r/w	0000 0000	P1 interrupt mask	3-6
	P1TRIG	FF24	r/w	0000 0000	P1 interrupt trigger control	3-7
	GPOCTR0	FF25	r/w	1111 11 <u>xx</u>	gen purpose output control	3-8
	GPOCTR1	FF26	r/w	0000 11 <u>x</u> 1	gen purpose output control	3-9
	XISTAT0	FF27	r	<u>0</u> xxx x <u>00</u> x	ext interrupt 0 status	3-10
	XISTAT1	FF28	r	<u>0000 000</u> x	ext interrupt 1 status	3-11
	XISTAT2	FF29	r	<u>0000 000</u> x	ext interrupt 2 status	3-11
	reserved	FF2A-2E		xxxx xxxx		
B/D MUX	BDMUX	FF2F	r/w	0000 0000	B/D channel routing mux	3-12

Table 3-1 External Data Space Address Map

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	Table 3-1	External Data	Space Address	Мар	(continued)
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Data Space	Register Mnemonic	Address	Access	Default	Description	Page
Serial Port	SIOMODE	FF30	r/w	<u>0000</u> 0000	serial port mode	3-13
	SIOTB	FF31	w	n/a	serial port transmit buffer	3-14
	SIORB	FF32	r	XXXX XXXX	serial port receive buffer	3-14
	SIOTBL	FF33	r/w	<u>xxxx x</u> 000	serial port transmit length	3-15
	reserved	FF34–FF36		XXXX XXXX		
	SIOSTAT	FF37	r	<u>0000 00</u> 10	serial port status	3-15
	SIOMASK	FF38	r/w	<u>0000 00</u> 00	serial port interrupt mask	3-16
	SIOSRC	FF39	r	<u>0000 00</u> 00	serial port interrupt source	3-17
	reserved	FF3A–FF4C		XXXX XXXX		
	SPTMG	FFED	r/w	<u>xxxx</u> <u>xx</u> 00	serial port clock rate	3-17
Modulator	MODTST	FF4D	r/w	<u>xxx</u> 0 <u>x</u> 000	modulator test mode	3-18
	reserved	FF4E		xxxx xxxx		
RSSI	RSSISTAT	FF4F	r/w	0x <u>0</u> x xxxx	RSSI status	3-19
Dual-Tone	T1FR1	FF50	r/w	XXXX XXXX	tone 1 frequency	3-21
Generator	T1FR2	FF51	r/w	XXXX XXXX	tone 1 frequency	3-21
	T1FR3	FF52	r/w	XXXX XXXX	tone 1 frequency	3-21
	T1AR	FF53	r/w	XXXX XXXX	tone 1 amplitude	3-22
	TTAR	FF54	r/w	XXXX XXXX	transmit tone attenuation	3-24
	T2FR1	FF55	r/w	XXXX XXXX	tone 2 frequency	3-21
	T2FR2	FF56	r/w	XXXX XXXX	tone 2 frequency	3-21
	T2FR3	FF57	r/w	XXXX XXXX	tone 2 frequency	3-21
	T2AR	FF58	r/w	XXXX XXXX	tone 2 amplitude	3-22
	RTAR	FF59	r/w	XXXX XXXX	receive tone attenuation	3-24
ADPCM	TXATTN	FF5A	r/w	XXXX XXXX	transmit attenuation	3-25
Transcoder	RXATTN	FF5B	r/w	xxxx xxxx	receive attenuation	3-25
	DSPCTR	FF5C	r/w	<u>00</u> 00 0000	transcoder mode control	3-26
Noise	NSCTR	FF2E	r/w	000 <u>x</u> 0000	noise suppression threshold	3-27
Suppression	NSTHR	FF5D	r/w	<u>x</u> xxx xxxx	noise suppress mute length	3-28
	MUTE	FF5E	r/w	<u>x</u> xxx xxxx	noise suppression control	3-28
	reserved	FF5F		XXXX XXXX		
	unused	FF60–FFBF				
	JITCTR	FFC7	r/w	0000 0000	jitter detection control	3-29

CT2RXBUF0-5FFC0-FFC5rxxxx xxxxreceive buffers 0-53-30FormatterTXBUF0-5FFC0-FFC5wxxxx xxxxtransmit buffers 0-53-30DEVMODEFFC6r/w00xx xxxxdevice mode: CFP/CPP3-31RXTMGRFFC8r/w000x x000receive timing recovery3-32TXMUXFFC9r/wxxxx x011transmit frame control3-33RXMUXFFCAr/wxxxx x011transmit frame control3-34TXDISABFFCBwxxxx xx00SYNCD control3-36SYNCDCFFCCr/wxxxx xx00SYNCD control3-36RDATACFFCBwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w00xx xxx0transmit power control3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-38DXXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-30	Data Space	Register Mnemonic	Address	Access	Default	Description	Page
FormatterTXBUF0-5FFC0-FFC5wxxxx xxxxtransmit buffers 0-53-30DEVMODEFFC6r/w00xx xxxxdevice mode: CFP/CPP3-31RXTMGRFFC8r/w000x x000receive timing recovery3-32TXMUXFFC9r/wxxxx x011transmit frame control3-33RXMUXFFCAr/wxxxx x011transmit frame control3-34TXDISABFFCBwxxxx xx01transmit disable3-35SYNCDCFFCCr/wxxxx xx00SYNCD control3-36RDATACFFCBwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w0xxx xxx0frame sync control3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-39DTXCTRFFD2r/w0000 0000burst sync control3-39	CT2	RXBUF0–5	FFC0–FFC5	r	XXXX XXXX	receive buffers 0–5	3-30
DEVMODEFFC6r/w00xx xxxxdevice mode: CFP/CPP3-31RXTMGRFFC8r/w000x x000receive timing recovery3-32TXMUXFFC9r/wxxxx x011transmit frame control3-33RXMUXFFCAr/wxxxx x011receive frame control3-34TXDISABFFCBwxxxx xx01transmit disable3-35SYNCDCFFCCr/wxxxx xx0SYNCD control3-36RDATACFFCBwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w0xxx xxx0transmit power control3-37BVALIDFFCFr/w0xxx xxx0transmit power control3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-39DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40	Formatter	TXBUF0–5	FFC0–FFC5	w	xxxx xxxx	transmit buffers 0–5	3-30
RXTMGRFFC8r/w000x x000receive timing recovery3-32TXMUXFFC9r/wxxxx x011transmit frame control3-33RXMUXFFCAr/wxxxx 0011receive frame control3-34TXDISABFFCBwxxxx xx01transmit disable3-35SYNCDCFFCCr/wxxxx xx0SYNCD control3-36RDATACFFCDwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w0xx xxxxenable B channel3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00transmit control3-39DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		DEVMODE	FFC6	r/w	00 <u>xx</u> <u>xxxx</u>	device mode: CFP/CPP	3-31
TXMUXFFC9r/wXXXX x011transmit frame control3-33RXMUXFFCAr/wXXXX 0011receive frame control3-34TXDISABFFCBwXXXX xx01transmit disable3-35SYNCDCFFCCr/wXXXX xx00SYNCD control3-36RDATACFFCDwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-36BVALIDFFCFr/w00xx xxx0transmit power control3-37SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wXXXX xx00D channel monitor control3-39DTXCTRFFD2r/w0000 0000burst sync control3-39SYNCFFD3r/w0000 0000burst sync control3-40		RXTMGR	FFC8	r/w	000 <u>x x</u> 000	receive timing recovery	3-32
RXMUXFFCAr/wxxxx 0011receive frame control3-34TXDISABFFCBwxxxx xx01transmit disable3-35SYNCDCFFCCr/wxxxx xx0SYNCD control3-36RDATACFFCDwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w00xx xxx0transmit power control3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-39DTXCTRFFD2r/w0000 0000burst sync control3-40		TXMUX	FFC9	r/w	<u>xxxx x</u> 011	transmit frame control	3-33
TXDISABFFCBwxxxx xx01transmit disable3-35SYNCDCFFCCr/wxxxx xx0SYNCD control3-36RDATACFFCDwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w0xxx xxxxenable B channel3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-39DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		RXMUX	FFCA	r/w	<u>xxxx</u> 0011	receive frame control	3-34
SYNCDCFFCCr/wxxxx xxx0SYNCD control3-36RDATACFFCDwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-36BVALIDFFCFr/w00xx xxx0transmit power control3-37SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-38DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		TXDISAB	FFCB	w	<u>xxxx xx</u> 01	transmit disable	3-35
RDATACFFCDwn/areceive data control3-36TPOWERFFCEr/w00xx xxx0transmit power control3-37BVALIDFFCFr/w0xxx xxxxenable B channel3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-39DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		SYNCDC	FFCC	r/w	<u>xxxx xxx</u> 0	SYNCD control	3-36
TPOWER BVALIDFFCE FFCFr/w00xx xxx0 0xxx xxx1transmit power control 		RDATAC	FFCD	w	n/a	receive data control	3-36
BVALIDFFCFr/w0xxx xxxxenable B channel3-38SYNCTRFFD0wn/aframe sync control3-38DMONITFFD1r/wxxxx xx00D channel monitor control3-38DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		TPOWER	FFCE	r/w	00 <u>xx</u> <u>xxx</u> 0	transmit power control	3-37
SYNCTRFFD0wn/aframe sync control3-36DMONITFFD1r/wxxxx xx00D channel monitor control3-38DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		BVALID	FFCF	r/w	0 <u>xxx xxxx</u>	enable B channel	2 20
DMONITFFD1r/wxxxx xx00D channel monitor control3-30DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		SYNCTR	FFD0	W	n/a	frame sync control	2.20
DTXCTRFFD2r/wxxxx xx00transmit control3-39BSYNCFFD3r/w0000 0000burst sync control3-40		DMONIT	FFD1	r/w	<u>xxxx xx</u> 00	D channel monitor control	3-30
BSYNC FFD3 r/w 0000 0000 burst svnc control 3-40		DTXCTR	FFD2	r/w	<u>xxxx xx</u> 00	transmit control	3-39
		BSYNC	FFD3	r/w	0000 0000	burst sync control	3-40
TDELAY FFD4 r/w 1000 1011 transmit delay control 3-41		TDELAY	FFD4	r/w	1000 1011	transmit delay control	3-41
RDELAY FFD5 r/w x000 1011 receive delay control ³⁻⁴²		RDELAY	FFD5	r/w	x000 1011	receive delay control	3-42
reserved FFD6–FFDC xxxx xxxx ³⁻⁴³		reserved	FFD6–FFDC		XXXX XXXX		3-43
MODTMG FFDD r/w xxxx xx00 modem timing adjustment		MODTMG	FFDD	r/w	<u>xxxx xx</u> 00	modem timing adjustment	
MODDLY FFDE r/w <u>x</u> 000 0000 modem delay register ³⁻⁴⁴		MODDLY	FFDE	r/w	<u>x</u> 000 0000	modem delay register	3-44
reserved FFDF xxxx xxxx 3-45		reserved	FFDF		XXXX XXXX		3-45
DCHSTAT FFE4 r <u>0</u> 000 0100 D channel interrupt status		DCHSTAT	FFE4	r	<u>0</u> 000 0100	D channel interrupt status	
CMSSRC FFE5 r <u>xxxx</u> 0000 CHM/SYNC interrupt source 3-46		CMSSRC	FFE5	r	<u>xxxx</u> 0000	CHM/SYNC interrupt source	3-46
CMSMASK FFE6 r/w xxxx 0000 CHM/SYNC interrupt mask 3-48		CMSMASK	FFE6	r/w	<u>xxxx</u> 0000	CHM/SYNC interrupt mask	3-48
3-49							3-49
Interrupt MISRC0 FFE0 r <u>00</u> 00 0000 main interrupt source 0 3-50	Interrupt	MISRC0	FFE0	r	<u>00</u> 00 0000	main interrupt source 0	3-50
Controller MISRC1 FFE1 r <u>0</u> 000 0000 main interrupt source 1 3-52	Controller	MISRC1	FFE1	r	<u>0</u> 000 0000	main interrupt source 1	3-52
MIMSK0 FFE2 r/w <u>00</u> 00 0000 main interrupt mask 0 3-53		MIMSK0	FFE2	r/w	<u>00</u> 00 0000	main interrupt mask 0	3-53
MIMSK1 FFE3 r/w 0000 0000 main interrupt mask 1 3-53		MIMSK1	FFE3	r/w	<u>0</u> 000 00 <u>0</u> 0	main interrupt mask 1	3-53
reserved FFE7–FFE8 xxxx xxxx		reserved	FFE7–FFE8		XXXX XXXX		
Clock UCCCTR FFE9 r/w 00xx x000 8032 clock, shutdown 3-54	Clock	UCCCTR	FFE9	r/w	00 <u>xx</u> <u>x</u> 000	8032 clock, shutdown	3-54
Generator UCCCP FFEA w n/a 8032 clock, shutdown 3-55	Generator	UCCCP	FFEA	w	n/a	8032 clock, shutdown	3-55
MECTR0 FFEB r/w <u>x0x0 xx00</u> module enable control 0 3-56		MECTR0	FFEB	r/w	<u>x0x</u> 0 <u>xx</u> 00	module enable control 0	3-56
MECTR1 FFEC r/w xx00 00x0 module enable control 1 3-57		MECTR1	FFEC	r/w	<u>xx</u> 00 00 <u>x</u> 0	module enable control 1	3-57
* FFED r/w (see Serial Port)		*	FFED	r/w		(see Serial Port)	-
reserved FFEE xxxx xxxx		reserved	FFEE		хххх хххх		
Watchdog WDTKEY FFEF w n/a WDT key register 3-58	Watchdog	WDTKEY	FFEF	W	n/a	WDT key register	3-58
Timer reserved FFF0-FFF	Timer	reserved	FFF0-FFFF				

Table 3-1 **External Data Space Address Map (continued)**

3.1.1 Reserved Register Bits

Many of the registers contain data fields that are reserved by AMD for feature enhancement in future silicon revisions. New features will be enabled by programming reserved bits High. For software compatibility with future silicon revisions, users must write zeroes to reserved data fields.

Except where noted, reads of reserved data fields return unknown values.

Read-modify-write operations may, in general, write back to the reserved field the value read.

Exceptions are noted in the individual register descriptions.

3.1.2 ADRDEC

Full name:	address decoder control register
Address:	FF0F
Default:	<u>0xxx xx</u> 0 <u>1</u>
Access:	read/write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
reserved	reserved	reserved	reserved	reserved	reserved	CS2	reserved		
						CPUCLK			
						SELECT			
Bit 7:	Reserved Important Note: Defaults to 0. Software must write 1.								
Bits 6–2:	Reserved								
Bit 1:	CS2_CP	S2_CPUCLK Select							
	This bit controls the function of the $\overline{CS2}$ _CPUCLK pin, depending on the								
	device mode, as shown in Table 3-2.								
Bit 0:	Reserved Important Note: Defaults to 1. Software must write 1.								

Table 3-2 CS2_CPUCLK Pin Configuration

CS2_CPUCLK SELECT	Emulation Mode	CS2_CPUCLK Pin Function	Description
0	No	CS2	Address decode output, for range F400–F7FF
1	No	CPUCLK	8032 clock output
x	Yes	CPUCLK	8032 clock output
3.2 PARALLEL PORT

3.2.1 P1SRC0

Full name:	P1 Interrupt Source Register 0
Address:	FF20
Default:	<u>0000 00</u> 00
Access:	read only

P1SRC0 latches occurrences of unmasked transitions on port pins P1.0 and P1.1 and generates the P1 INT 0 interrupt reported in MISRC1[4]. Each bit is:

- Set by a P1 transition if the associated bit in P1MASK is set. The polarity of the transition is defined by the P1TRIG register.
- Cleared by reading P1SRC0 or by applying reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	P1.1	P1.0
						INTRUPT	INTRUPT
						FLAG	FLAG

Bits 7–2:Reserved. Reads return zeroes, subject to change in future silicon revisions.Bit 1:P1.1 Interrupt Flag

Bit 0: P1.0 Interrupt Flag

3.2.2 P1SRC1

Full name:	P1 Interrupt Source Register 1
Address:	FF21
Default:	<u>0000 00</u> 00
Access:	read only

P1SRC1 latches occurrences of unmasked transitions on port pins P1.2 and P1.3 and generates the P1 INT 1 interrupt reported in MISRC1[5]. Each bit is:

- Set by a P1 transition if the associated bit in P1MASK is set. The polarity of the transition is defined by the P1TRIG register.
- Cleared by reading P1SRC1 or by applying reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	P1.3	P1.2
						INTRUPT	INTRUPT
						FLAG	FLAG

Bits 7–2:Reserved. Reads return zeroes, subject to change in future silicon revisions.Bit 1:P1.3 Interrupt Flag

Bit 0: P1.2 Interrupt Flag

3.2.3 P1SRC2

Full name:	P1 Interrupt Source Register 2
Address:	FF22
Default:	<u>0000</u> 0000
Access:	read only
	Bit 6 has read/write access

P1SRC2 latches occurrences of unmasked transitions on port pins P1.4–P1.7 and generates the P1 INT 2 interrupt reported in MISRC1[6]. Each bit is:

- Set by a P1 transition if the associated bit in P1MASK is set. The polarity of the transition is defined by the P1TRIG register.
- Cleared by reading P1SRC2 or by applying reset.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	ENSYNC_I/O	reserved	reserved	P1.7	P1.6	P1.5	P1.4
				INTRUPT	INTRUPT	INTRUPT	INTRUPT
				FLAG	FLAG	FLAG	FLAG

Bits 7, 5, 4: Reserved. Reads return zeroes, subject to change in future silicon revisions.

- Bit 6: Enable Sync I/O allows the P1.6 pin to be used as a 500-Hz CT2 frame sync input or output. In either case, port P1.6 can still be read by the 8032 and can trigger the interrupt flagged in bit 2.
 - 0: Disable pin P1.6 as a 500-Hz sync port
 - 1: Enable pin P1.6 as a 500-Hz sync port
- Bit 3: P1.7 Interrupt Flag
- Bit 2: P1.6 Interrupt Flag
- Bit 1: P1.5 Interrupt Flag
- Bit 0: P1.4 Interrupt Flag

3.2.4 P1MASK

Full name:	P1 Interrupt Mask Register
Address:	FF23
Default:	0000 0000
Access:	read/write

P1MASK individually masks transitions on P1 bits affecting P1SRC2–P1SRC0. For all bits:

- 0: Disable interrupt source and clear corresponding source bit
 - 1: Enable corresponding interrupt source

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
INTRUPT							
MASK							

3.2.5 P1TRIG

Full name:P1 Interrupt Trigger RegisterAddress:FF24Default:0000 0000Access:read/write

P1TRIG defines the polarity of transitions on individual P1 bits, causing interrupts to be latched in the P1SRC2–P1SRC0 registers. For all bits:

- 0: High-to-Low transitions cause interrupts.
- 1: Low-to-High transitions cause interrupts.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
TRIG							
SELECT							

3.2.6 GPOCTR0

Full name:General-Purpose Output Control Register 0Address:FF25Default:1111 11xxAccess:read/write

GPOCTR0 controls the general-purpose outputs OUT7–OUT2, which are outputs on multifunction pins configured by the BDMUX register, bits [6:5], and by GPOCTR1[6:5]. Values written to GPOCTR0 are internally latched regardless of whether a pin is configured for OUT operation, and are driven on the pin only when the pin is appropriately configured.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	reserved	reserved	
Bit 7:	OUT7, en 0: OUT 1: OUT	abled on th 7 drives Lo 7 drives Hi	e OUT7 pir ow gh	n if GPOCT	R1[6]=1			
Bit 6:	OUT6, enabled on the OUT6 pin if GPOCTR1[5]=1 0: OUT6 drives Low 1: OUT6 drives High							
Bit 5:	OUT5, enabled on the BDP3_OUT5 pin if BDMUX[6:5]=01 0: OUT5 drives Low 1: OUT5 drives High							
Bit 4:	OUT4, enabled on the BDP2_OUT4 pin if BDMUX[6:5]=01 0: OUT4 drives Low 1: OUT4 drives High							
Bit 3:	OUT3, enabled on the BDP1_OUT3 pin if BDMUX[6:5]=01 0: OUT3 drives Low 1: OUT3 drives High							
Bit 2:	OUT2, en 0: OUT 1: OUT	abled on th 2 drives Lo 2 drives Hi	e BDP0_O w gh	UT2 pin if E	BDMUX[6:5]=01		

Bits 1–0: Reserved

3.2.7 **GPOCTR1**

Full name:	General-Purpose Output Control Register 1
Address:	FF26
Default:	0000 11 <u>x</u> 1
Access:	read/write

GPOCTR1 controls the general-purpose outputs OUT8, OUT10, and OUT11, which are outputs on multifunction pins configured by the BDMUX register, bit 7, and by GPOCTR1[7]. Values written to GPOCTR1[3:0] are latched regardless of whether a pin is configured for OUT operation or not.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRI0_ OUT10 SELECT	OUT7 ENABLE	OUT6 ENABLE	reserved	OUT11	OUT10	reserved	OUT8

Bit 7: TRI0_OUT10 Select

- 0: The TRI0_OUT10 pin is the TRI0 input (tri-level input 0).
- 1: The TRI0_OUT10 pin is the OUT10 output.

Bit 6: OUT7 Enable

- 0: Disable output OUT7. Pin is weakly pulled High.
- 1: The OUT7 pin is driven by the value programmed in GPOCTR0[7]

Bit 5: OUT6 Enable

- 0: Disable output OUT6. Pin is weakly pulled High.
- 1: The OUT6 pin is driven by the value programmed in GPOCTR0[6]
- Bit 4: Reserved
- Bit 3: OUT11, enabled on the BDP5_OUT11 pin when BDMUX[7] is High
 - 0: OUT11 drives Low
 - 1: OUT11 drives High
- Bit 2: OUT10, enabled on the TRI0_OUT10 pin when GPOCTR1[7] is High
 - 0: OUT10 drives Low
 - 1: OUT10 drives High
- Bit 1: Reserved
- Bit 0: OUT8, enabled on the BDP4_OUT8 pin when BDMUX[7] is High
 - 0: OUT8 drives Low
 - 1: OUT8 drives High

3.2.8 XISTATO

Full name:TRI0, TRI1, and External Interrupt 0 Status RegisterAddress:FF27Default:0xxx x00xAccess:read only

XISTAT0 reports the current logic levels of TRI0, TRI1, and XINT0 pins.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	TF	RI1	TF	RIO	reserved	reserved	EXINT0

Bit 7: Reserved. The current silicon revision returns zeroes; subject to change in future revisions.

Bits 6–5: TRI1 Pin Level

- 00: Open or mid-supply (basic mode = Customer Test Mode)
- 01: Low (basic mode = Emulation)
- 10: High (basic mode = Normal)
- 11: Reserved, not used

Bits 4–3: TRI0 Pin Level

- 00: Open or mid-supply
- 01: Low
- 10: High
- 11: Reserved, not used
- Bits 2–1: Reserved. The current silicon revision returns zeroes; subject to change in future revisions.
- Bit 0: XINT0 Pin Level
 - 0: XINT0 pin is Low
 - 1: XINT0 pin is High

3.2.9 XISTAT1

Full name:External Interrupt 1 Status RegisterAddress:FF28Default:0000 000xAccess:read only

XISTAT1 reports the current logic level of the XINT1 pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	XINT1						

- Bits 7–1: Reserved. The current silicon revision returns zeroes; subject to change in future revisions.
- Bit 0: XINT1 Pin Level

0:

- XINT1 pin is Low
- 1: XINT1 pin is High

3.2.10 XISTAT2

Full name:	External Interrupt 2 Status Register
Address:	FF29
Default:	<u>0000</u> 000x
Access:	read only

XISTAT2 reports the current logic level of the XINT2 pin.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	XINT2						

Bits 7–1: Reserved. The current silicon revision returns zeroes; subject to change in future revisions.

- Bit 0: XINT2 Pin Level
 - 0: XINT2 pin is Low
 - 1: XINT2 pin is High

3.3 BDMUX

Full name: Address: Default: Access: B/D Channel Port Multiplexer Control Register FF2F 0000 0000 read/write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENC_OUT SELECT	PIN SI	ELECT	B CH PORT TX SRC	CT2 TX B SOU	CHANNEL IRCE	ADPCM	SOURCE

Bit 7: Encryption/General-Purpose Output Selection

- 0: The BDP5_OUT11 pin serves the BDP5 function, which is 32-kbps transmit encryption input (TXENCIN). The BDP4_OUT8 pin serves the BDP4 function, which is 32-kbps receive encryption output (RXENCOUT).
- 1: The BDP5_OUT11 pin serves the OUT11 function and the BDP4_OUT8 pin serves the OUT8 function.
- Bits 6–5: PIN SELECT[1:0] controls the configuration of four multifunction pins, described in Table 3-3.
- Bit 4: B Channel Port Transmit Source
 - 0: 32-kbps B channel output (BCHOUT) on BDP0_OUT2 follows the transmit ADPCM output if BDMUX[6:5] = 00.
 - 1: BCHOUT follows the unscrambled received CT2 B channel if BDMUX[6:5] = 00.
- Bits 3–2: The CT2 Transmit B Channel Source identifies the B channel data to be transmitted over the radio link.
 - 00: Transmit ADPCM output.
 - 01: BCHIN on the BDP1_OUT3 pin if BDMUX[6:5] = 00. If BDMUX[6:5] \neq 00, operation is unpredictable.
 - 10: Unscramble received CT2 B channel (i.e., Loopback 3)
 - 11: TXENCIN on the BDP5_OUT11 pin
- Bits 1–0: ADPCM Receiver Source
 - 00: CT2 receive B channel
 - 01: BDATAIN on the BDP1_OUT3 pin if BDMUX[6:5] = 00. If BDMUX[6:5] \neq 00, operation is unpredictable.
 - 10: Codec transmit ADPCM output (i.e., Loopback 1)
 - 11: Hexadecimal 0

Table 3-3 PIN SELECT Multifunction Pin Configuration

BDMUX [6:5]	Mnemonic	BDP0_OUT2 pin	BDP1_OUT3 pin	BDP2_OUT4 pin	BDP3_OUT5 pin	Section Ref
00	B Channel	BCHOUT	BCHIN	BCLK	CLK8K	2.4.3
01	Gen-Purpose Outputs	OUT2	OUT3	OUT4	OUT5	2.2.6
10	D Channel	DCT2RX	DTXDATAIO	DRXCLK	DTXCLK	2.5.2
11	CT2 Transmit	CT2TXCLK	CT2TXD	CT2TXEN	CLK8K	2.3.1.12

3.4 SERIAL PORT

3.4.1 SIOMODE

Full name:	Serial Port Mode
Address:	FF30
Default:	<u>0000</u> 0000
Access:	read/write

SIOMODE defines serial port sequence and timing. Refer to Figures 2-2 through 2-6.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	CLOCK	RX	RX	READ/
				LEVEL	CLOCK	WORD	WRITE
				SELECT	EDGE	LENGTH	

Bits 7–4: Reserved

Bit 3: Clock Active Level Select

- 0: Active Low clock (i.e., SCLK=1 when no transmission/reception is active)
- 1: Active High clock (i.e., SCLK=0 when no transmission/reception is active)

Bit 2: Receive Clock Edge

- 0: Receive data on SIODIN is latched on High-to-Low transition of SCLK
- 1: Receive data on SIODIN is latched on Low-to-High transition of SCLK
- Bit 1: Receive Data Length Select
 - 0: 16 bit
 - 1: 8 bit

Bit 0: Write/Write-Read Selection

- 0: Write-only sequence
- 1: Write-then-read sequence

3.4.2 SIOTB

Full name: Address: Default: Access:	2 F 1 \	Serial Port ⁻ F31 Not applical write only	Γransmit Βι ble	uffer			
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Writing SIOTB when the serial port is enabled (MECTR0[4]) starts a hardware write or write-read sequence and clears the transmit buffer empty interrupt. Software should allow no writes during transmission or reception.

SIOTB

The length of the data field is programmable from 1 to 8 bits and is defined in the SIOTBL (transmit buffer length) register. Data written to SIOTB is transmitted most significant bit first and must be right-justified in the register.

3.4.3 SIORB

Full name:	Serial Port Receive Buffer
Address:	FF32
Default:	XXXX XXXX
Access:	read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIORB							

SIORB is the serial port receive buffer, which is one or two bytes deep, depending on SIOMODE[1]. The receive buffer is loaded during the second part of the write-read sequence, enabled by SIOMODE[0]. Data is valid only after the SIOSTAT[0] or SIOSRC[0] bits indicate that receive data is available. If a second read operation is initiated before the buffer has been read, the buffer contents are overwritten with the new receive data.

For 8-Bit Receive Data:

A read returns the receive data byte. The receiver places the first received bit in the most significant position.

For 16-Bit Receive Data:

16-bit data operations require two reads, both subject to the requirement that the receive data available indicator is true. The first read returns the first byte received, most significant bit first, and may be read after the first 8 bits have been received. The second read operation returns the second byte received.

3.4.4 SIOTBL

Full name:	Serial Port Transmit Buffer Length
Address:	FF33
Default:	<u>xxxx x</u> 000
Access:	read/write

SIOTBL defines the number of transmit buffer bits transmitted.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	TRANSMIT BUFFER LENGTH		

Bits 7–3: Reserved

Bits 2–0:	Transmit Buffer	Length
	000: 8 bits	100: 4 bits
	001: 1 bit	101: 5 bits
	010: 2 bits	110: 6 bits
	011: 3 bits	111: 7 bits

3.4.5 SIOSTAT

Serial Port Status
FF37
<u>0000 00</u> 10
read only

SIOSTAT contains the unmasked status of the transmit buffer empty and receive data available indicators.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	TX BUFFER EMPTY	RX BUFFER FULL

Bits 7–2: Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1: Transmit Buffer Empty Status

- 0: The transmit buffer is not empty (default state).
- 1: The transmit buffer is empty.
- Bit 0: Receive Data Available Status
 - 0: No valid data is in the receive buffer.
 - 1: Valid data is in the receive buffer. For 16-bit reads, this bit becomes true when the first 8 bits are received and again when the 16th bit is received.

3.4.6 SIOMASK

Full name:Serial Port Interrupt MaskAddress:FF38Default:0000 0000Access:read/write

The SIOMASK interrupt mask lies between the status and source registers. Status bits are logically ANDed with mask bits to yield source bits.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	TX BUFFER EMPTY MASK	RX BUFFER FULL MASK

Bits 7–2: Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1: Transmit Buffer Empty Interrupt Mask

- 0: Transmit buffer empty interrupt disabled
- 1: Transmit buffer empty interrupt enabled

Important Note: In typical applications, software should set this bit only after transmission has begun (i.e., after SIOTB is written).

Bit 0: Receive Data Available Status

- 0: Receive data available interrupt disabled
- 1: Receive data available interrupt enabled

3.4.7 SIOSRC

Full name:Serial Port Interrupt SourceAddress:FF39Default:0000 0000Access:read/write

SIOSRC contains the masked status of the transmit buffer empty and receive data available indicators.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	TX BUFFER EMPTY	RX BUFFER FULL
						FLAG	FLAG

Bits 7–2: Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 1: Transmit Buffer Empty Flag

- 0: The transmit buffer is not empty or SIOMASK[1]=0.
- 1: The transmit buffer is empty and SIOMASK[1]=1.
- Bit 0: Receive Data Available Flag
 - 0: No valid data is in the receive buffer or SIOMASK[0]=0.
 - 1: Valid data is in the receive buffer and SIOMASK[0]=1.

3.4.8 SPTMG

Full name:	Serial Port Timing Control Register
Address:	FFED
Default:	<u>xxxx xx</u> 00
Access:	read/write

SPTMG specifies the clock rate of the serial port enabled by MECTR0[4]. The serial port clock appears on the SCLK pin. To avoid unpredictable clock pulses, software should reprogram bits only when the serial port is disabled.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	SERIAL PORT CLOCK RATE CONTROL	

Bits 7-2: Reserved

Bits 1–0: Serial Port Clock Rate Control

00: Selected SCLK output rate is 36 kHz

- 01: Selected SCLK output rate is 72 kHz
- 10: Selected SCLK output rate is 144 kHz
- 11: Selected SCLK output rate is 288 kHz

3.4.9 MODTST

Full name: Address:	Modulator Test Mode Register
Default:	<u>xxx0_x000</u>
Access:	read/write

MODTST enables constant transmission modes for the CT2 Baseband Output Driver for the purpose of spectral measurement. When in test mode, the modulator ignores the CT2 Formatter data and transmits instead either an internally generated fixed pattern or arbitrary data from an external source. To use the external source, BDMUX[6:5] must be programmed to 11. The external source drives data on the BDP1_OUT3 pin, clocked by rising edges of the 72-kHz clock output on the BDP0_OUT2 pin. The modulator must be enabled in MECTR1[4] in order to function.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	NRZ/IQ	reserved	MOD TEST	TEST	MODE
					ENABLE		

Bits 7–5: Reserved

- Bit 4: I/Q/NRZ Data Output Format
 - 0: I/Q analog output
 - 1: NRZ quasi-digital output
- Bit 3: Reserved
- Bit 2: Modulator Test Enable
 - 0: Disable test mode, (i.e., normal mode)
 - 1: Enable test mode
- Bits 1–0: Modulator Test Mode
 - 00: Transmit all 0s (i.e., $\omega_m(t) = \omega_{min} = -2\pi \cdot 18$ kHz for I/Q format)
 - 01: Transmit data from external source
 - 10: Transmit alternating 1s and 0s (i.e., $\omega_m(t)$ varies over = $\pm 2\pi \cdot 18$ kHz for I/Q format)
 - 11: Transmit all 1s (i.e., $\omega_m(t) = \omega_{max} = + 2\pi \cdot 18$ kHz for I/Q format)

3.4.10 RSSISTAT

Full name:	RSSI Status Register
Address:	FF4F
Default:	0x <u>0</u> x xxxx
Access:	read/write

RSSISTAT reports the result of the RSSI A/D conversion of the voltage at the RSSI pin. Setting bit 7 requests a conversion. Software polls RSSISTAT until bit 7 is cleared by hardware, indicating that the conversion is complete and bits 4–0 have a valid code. Bit 6 reports the status of microcontroller port pin P1.7, allowing a simultaneous read of the RSSI level and some arbitrary digital input, such as one reporting channel status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSSI	P1.7	reserved	RSSI				
REQUEST	STATUS		VALUE				

Bit 7: RSSI Request

- 0: (read) conversion complete
- 1: (write) conversion request, (read) conversion not complete
- Bit 6: Microcontroller Port Pin P1.7 Status (read only)
 - Pin P1.7 may be used to monitor the free channel status signal.
 - 0: P1.7 is 0
 - 1: P1.7 is 1
- Bit 5: Reserved. Software must write zero. Reads return zeroes, subject to change in future silicon revisions.

Bits 4–0: RSSI Value These five bits report the result of the A/D conversion, listed in Table 3-4.

Table 3-4 RSSI Codes

RSSISTAT 4–0	Nominal Center Voltage	RSSISTAT 4–0	Nominal Center Voltage
0 0000	0.220	1 0000	0.760
0 0001	0.253	1 0001	0.794
0 0010	0.287	1 0010	0.828
0 0011	0.321	1 0011	0.861
0 0100	0.355	1 0100	0.895
0 0101	0.389	1 0101	0.929
0 0110	0.422	1 0110	0.963
0 0111	0.456	1 0111	0.997
0 1000	0.490	1 1000	1.030
0 1001	0.524	1 1001	1.064
0 1010	0.557	1 1010	1.098
0 1011	0.591	1 1011	1.132
0 1100	0.625	1 1100	1.166
0 1101	0.659	1 1101	1.199
0 1110	0.693	1 1110	1.233
0 1111	0.726	1 1111	1.267

3.5 DUAL-TONE GENERATOR

3.5.1 T1FR1-3,T2FR1-3 (Dual-Tone Frequency)

T1FR1–T1FR3 (Tone 1 Frequency Registers 1 through 3) and T2FR1–T2FR3 control the frequency of the first and second tones, respectively, from the dual-tone generator. They are actually RAM locations that reset to indeterminate states and therefore must be initial-ized before the codec block is enabled.

All dual-tone generator values (i.e., data space FF50–FF59) are double-buffered and progress to the ADPCM transcoder RAM simultaneously, keyed by a write to the RTAR location (address FF59). Therefore, if a change in any DTMF-related value is required, the write sequence must conclude with a write to RTAR.

Figure 3-1 is a short-form listing of standard DTMF tones. Appendix A is a full list of valid values in order of increasing frequency.

Mnemonic	Address
T1FR1	FF50
T1FR2	FF51
T1FR3	FF52
T2FR1	FF55
T2FR2	FF56
T2FR3	FF57

Figure 3-1 DTMF Frequency Short-Form

		Tone 2 \rightarrow	1209 Hz	1336 Hz	1477 Hz	1633 Hz
		T2FR1-3 \rightarrow	98 40 4A	91 62 3F	8B 0E 33	85 31 24
			\checkmark	\checkmark	\checkmark	\downarrow
Tone 1 \downarrow	T1FR1–3 ↓		\checkmark	\downarrow	\downarrow	\downarrow
697 Hz	BD 26 6D	\rightarrow \rightarrow	1	2	3	Α
770 Hz	B7 26 69	\rightarrow \rightarrow	4	5	6	В
852 Hz	B1 33 64	\rightarrow \rightarrow	7	8	9	С
941 Hz	AA 4D 5E	\rightarrow \rightarrow	*	0	#	D

4 x 4 Keypad

18515A-40

3.5.2 T1AR, T2AR (Dual-Tone Amplitude)

T1AR (Tone 1 Amplitude Register) and T2AR control the amplitudes of the first and second tones, respectively, from the dual-tone generator. After application of the programmed gains, the two tones are summed; therefore, gains should be programmed so that the sum of the two tones does not cause the digital signal processor accumulator to overflow, resulting in clipping. T1AR and T2AR are RAM locations that reset to indeterminate states and therefore must be initialized before the codec block is enabled.

All dual-tone generator values (i.e., data space FF50–FF59) are double-buffered and progress to the ADPCM transcoder RAM simultaneously, keyed by a write to the RTAR location (address FF59). Therefore, if a change in any dual-tone generator value is required, the write sequence must conclude with a write to RTAR.

Table 3-5 lists valid values.

Mnemonic	Address
T1AR	FF53
T2AR	FF58

Code	Attenuation (dB)	Code	Attenuation (dB)	Code	Attenuation (dB)
00	No Output	30	-8.52	60	-3.50
01	-42.14	31	-8.34	61	-2.41
02	-36.12	32	-8.16	62	-2.32
03	-32.60	33	-7.99	63	-2.23
04	-30.10	34	-7.82	64	-2.14
05	-28.16	35	-7.66	65	-2.06
06	-26.58	36	-7.50	66	-1.97
07	-25.24	37	-7.34	67	-1.89
08	-24.08	38	-7.18	68	-1.80
09	-23.06	39	-7.03	69	-1.72
0a	-22.14	3a	-6.88	6a	-1.64
0b	-21.32	3b	-6.73	6b	-1.56
0c	-20.56	3c	-6.58	6c	-1.48
0d	-19.87	3d	-6.44	6d	-1.40
0e	-19.22	3e	-6.30	6e	-1.32
Of	-18.62	3f	-6.16	6f	-1.24
10	-18.06	40	-6.02	70	-1.16
11	-17.54	41	-5.89	71	-1.08
12	-17.04	42	-5.75	72	-1.01
13	-16.57	43	-5.62	73	-0.93
14	-16.12	44	-5.49	74	-0.86
15	-15.70	45	-5.37	75	-0.78
16	-15.30	46	-5.24	76	-0.71
17	-14.91	47	-5.12	77	-0.63
18	-14.54	48	-5.00	78	-0.56
19	-14.19	49	-4.88	79	-0.49
la	-13.84	4a	-4.76	7a	-0.42
lb	-13.52	4b	-4.64	7b	-0.35
lc	-13.20	4c	-4.53	7c	-0.28
1d	-12.90	4d	-4.41	7d	-0.21
1e	-12.60	4e	-4.30	7e	-0.14
1f	-12.32	4f	-4.19	7f	-0.07
20	-12.04	50	-4.08		
21	-11.77	51	-3.97		
22	-11.51	52	-3.87		
23	-11.26	53	-3.76		
24	-11.02	54	-3.66		
25	-10.78	55	-3.56		
26	-10.35	56	-3.45		
27	-10.32	57	-3.35		
28	-10.10	58	-3.25		
29	-9.89	59	-3.16		
2a	-9.68	5a	-3.06		
2b	-9.47	5b	-2.96		
2c	-9.28	5c	-2.87		
2d	-9.08	5d	-2.77		
2e	-8.89	5e	-2.68		
2f	-8.70	5f	-2.59		

Table 3-5 Attenuation Codes—Valid for T1AR, T2AR, RTAR, TTAR, RXATTN, and TXATTN

3.5.3 TTAR, RTAR (Dual-Tone Path Attenuation)

TTAR (Transmit Tone Attenuation Register) and RTAR (Receive Tone Attenuation Register) control the level of the dual-tone signal in the transmit and receive data paths, respectively. After application of the programmed attenuation, the dual-tone signal is summed with audio data; therefore, attenuations should be programmed so that the sum of the dual-tone signal and audio data does not cause the codec accumulator to overflow, resulting in clipping. TTAR and RTAR are RAM locations that reset to indeterminate states and therefore must be initialized before the codec block is enabled.

All dual-tone generator values (i.e., data space FF50–FF59) are double-buffered and progress to the ADPCM transcoder RAM simultaneously, keyed by a write to the RTAR location (address FF59). Therefore, if a change in any dual-tone generator value is required, the write sequence must conclude with a write to RTAR.

Table 3-5 lists valid values.

Mnemonic	Address
TTAR	FF54
RTAR	FF59

3.6 ADPCM TRANSCODER

3.6.1 **TXATTN**

Full name:	Transmit Attenuation
Address:	FF5A
Default:	XXXX XXXX
Access:	read/write

The TXATTN byte controls the attenuation applied to the transmitted B channel data. It is a RAM location that must be initialized before the codec is enabled. Codes are tabulated in Table 3-5.

3.6.2 RXATTN

Full name:	Receive Attenuation
Address:	FF5B
Default:	XXXX XXXX
Access:	read/write

The RXATTN byte controls the attenuation applied to the received B channel data. It is a RAM location that must be initialized before the codec is enabled. Codes are tabulated in Table 3-5.

3.6.3 DSPCTR

Full name:Digital Signal Processor Control RegisterAddress:FF5CDefault:0000 0000Access:read/write

DSPCTR controls the operating mode of the codec when it is enabled by MECTR0[6]. To avoid unpredictable results, software must disable the codec by clearing MECTR0[6] before changing DSPCTR.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	NOISE	ATTN		TRANS	CODER	
		SUPPR	ENABLE/		PA	TH	
		ENABLE	BYPASS				

Bits 7–6: Reserved

Bit 5: Noise Suppression Enable

- 0: Noise suppression algorithm is disabled.
- 1: Enable noise suppression, further controlled in NSCTR, NSTHR, MUTE, and JITCTR registers.
- Bit 4: Attenuation Enable/Bypass Control Bypassing the attenuators allows bit-for-bit compliance with CCITT G.721 using the sequences recommended by CCITT.
 - 0: Bypass attenuators TXATTN and RXATTN.
 - 1: Enable attenuators TXATTN and TXATTN.

Bits 3–0: Transcoder Path Control These bits determine the PCM I/O format for the ADPCM transcoder. Codes not listed are reserved. 0100: A-law ADPCM transcoder configuration

1100: μ-law ADPCM transcoder configuration

3.7 NOISE SUPPRESSION

3.7.1 **NSCTR**

Full name:	Noise Suppression Control Register
Address:	FF2E
Default:	000 <u>x</u> 0000
Access:	read/write

NSCTR controls the behavior of the noise suppression algorithm.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
JITTER STATUS	DSP NOISE STATUS	DSPINT EN	reserved	MUTE	MODE	MUTE	STEP

Bit 7: Jitter Status

- Read only. Set by a jitter detection trigger. Cleared by reading the register.
- 1: Jitter has occurred on the CT2 link, as defined by the JITTER register, since this register was last read.
- 0: No jitter has occurred since the last read of this register.
- Bit 6: Noise Status

Read only. Active High if enabled in bit 5 and set by a DSP-based noise detection trigger. Cleared by reading the register.

- 0: No DSP-based noise trigger occurred since NSCTR was last read.
- 1: A DSP-based noise trigger occurred in the codec receiver since last read of NSCTR.
- Bit 5: Noise Interrupt Enable
 - 0: Noise interrupt and status indicator disabled.
 - 1: Enable the DSP Noise Status Bit (bit 6) and a corresponding interrupt reported in MISRC0[5] to indicate that a codec DSP-based noise trigger occurred, regardless of whether actual muting is enabled to occur.
- Bit 4: Reserved

Bits 3–2: Mute Mode

Applicable when noise suppression is enabled in DSPCTR[5].

- 00: Trigger mute sequence on DSP noise or jitter detection
- 01: Trigger mute sequence on DSP noise detection only
- 10: Trigger mute sequence on jitter detection only
- 11: Trigger mute sequence on concurrent DSP noise and jitter detection

Bits 1–0: Mute Sequence

Applicable when noise suppression is enabled. See Figure 2-18. A mute sequence is initiated when noise is detected, according to the Mute Mode bits above. Each attenuation step lasts a duration specified in the MUTE register. 00: Full Mute, 0 dB

- 00. Full Mute, 0 dB
- 01: Full Mute, –6 dB, 0 dB
- 10: Full Mute, -12 dB, -6 dB, 0 dB
- 11: Full Mute, -18 dB, -12 dB, -6 dB, 0 dB

3.7.2 **NSTHR**

Full name:	Noise Threshold
Address:	FF5D
Default:	<u>x</u> xxx xxxx
Access:	read/write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	THR [3]	THR [2]	THR [1]	THR [0]	THR [–1]	THR [–2]	THR [–3]

Bit 7: Reserved. Must be written to 0. Reads back the value written.

THR is a binary representation in the form $3 \ 2 \ 1 \ 0. -1 \ -2 \ -3.$ THR[3:0] is a whole number and THR[-1, -2,-3] forms the fractional part. For example, 9.75 dB is represented as NSTHR = 0 1001 110 (9 + 0.5 + 0.25)

The maximum is 15.875 dB.

3.7.3 MUTE

Full name:	Noise Suppression Mute Length
Address:	FF5E
Default:	<u>x</u> xxx xxxx
Access:	read/write

MUTE defines the length of muting steps in the noise suppression algorithm. It is a RAM location and therefore must be initialized before noise suppression is enabled.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved				MUTE	-	-	

Bit 7: Reserved. Must be written to 0. Reads back the value written.

Bits 6–0: MUTE[6:0] is a binary representation from 0 to 127 of the duration of the noise suppression attenuation steps in units of 125-µs frame periods.

Bits 6–0: The THR field sets the trigger level in dB for noise detected in the B channel. The noise detector calculates the ratio of predicted received signal to the difference between predicted and actual received signal and generates a muting trigger when the ratio falls below the programmed threshold. Therefore, increasing THR causes the mute mechanism to be more sensitive to noise but more likely to trigger on genuine non-noisy speech. Low values allow more tolerance.

3.7.4 JITCTR

Full name: Address: Default: Access: Jitter Detection Control Register FFC7 0000 0000 read/write

JITCTR determines the threshold for detecting jitter in the CT2 link for the purposes of link maintenance and B channel noise suppression.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	EVENT	THRSH			PHASE	THRSH	-

- Bits 7–4: The event threshold specifies the minimum number of jitter events that must occur during a frame to cause the noise suppression jitter trigger to become active according to Table 3-6.
- Bits 3–0: The phase threshold specifies in degrees relative to the expected receive bit boundary the amount of phase error that causes a jitter error event to be counted, listed in Table 3-7.

Table 3-6 Jitter Event Threshold Codes

EVENT THRSH 3 2 1 0	Jitter Events per 2-ms frame
0000	4
0001	8
0010	12
0011	16
0100	20
0101	24
0110	28
0111	32

EVENT THRSH 3 2 1 0	Jitter Events per 2-ms frame
1000	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Table 3-7 Jitter Phase Threshold Codes

PHASE THRSH 3 2 1 0	Phase Error (degrees)
0000	No errors reported
0001	±168.75
0010	±157.50
0011	±146.25
0100	±135.00
0101	±123.75
0110	±112.50
0111	±101.25

PHASE THRSH 3 2 1 0	Phase Error (degrees)
1000	±90.00
1001	±78.75
1010	±67.50
1011	±56.25
1100	±45.00
1101	±33.75
1110	±22.50
1111	±11.25

3.8 CT2 FORMATTER

3.8.1 RXBUF0-RXBUF5

Full name:	CT2 D Channel Receive Buffer (six byte						
Address:	RXBUF0	FFC0					
	RXBUF1	FFC1					
	RXBUF2	FFC2					
	RXBUF3	FFC3					
	RXBUF4	FFC4					
	RXBUF5	FFC5					
Default:	XXXX XXXX						
Access:	read only						

Received D channel data is stored in the receive buffer, starting with RXBUF0 bit 0 (corresponding to bit 1 of octet 1, in CT2 protocol terminology) and ending with RXBUF5 bit 7 (bit 8 of octet 6). The receive buffer full flag is set by hardware when the last bit of the code word is received. The flag is cleared by reading the most significant byte of the buffer (FFC5).

The receive buffer can retain either one or two complete code words, depending on DEVMODE[6].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			RXB	UFx			

3.8.2 TXBUF0-TXBUF5

Full name:	CT2 D Channel Transmit Buffer (six bytes					
Address:	TXBUF0	FFC0				
	TXBUF1	FFC1				
	TXBUF2	FFC2				
	TXBUF3	FFC3				
	TXBUF4	FFC4				
	TXBUF5	FFC5				
Default:	xxxx xxxx					
Access:	write only					

The six transmit buffer bytes are transmitted serially in the D channel, starting with TXBUF0 bit 0 (corresponding to bit 1 of octet 1 in CT2 protocol terminology) and ending with TXBUF5 bit 7 (bit 8 of octet 6). When the buffer is empty, as defined by the D Channel Transmit Control Register, the transmit buffer empty flag is set. Writing the last byte, TXBUF5, clears the flag.

The transmit buffer can be loaded with either one or two complete code words, depending on DEVMODE[6].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXBUFx							

3.8.3 DEVMODE

Full name:Device Mode Select RegisterAddress:FFC6Default:00xx xxxxAccess:read/write

DEVMODE defines the basic operation of the CT2 device as either a CFP or a CPP. The formatter must be in clear mode (program TXMUX[1:0]=11 and RXMUX[1:0]=11) to change the contents of this register with predictable results.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPP/CFP	DOUBLE BUFFER	reserved	reserved	reserved	reserved	reserved	reserved

Bit 7: CPP/CFP Mode Selection

- 0: The PhoX device operates as a CT2 Fixed Part (CFP).
- 1: The device operates as a CT2 Portable Part (CPP).

Bit 6: Double Buffer Enable and SYNCD Mode

0: Transmit and Receive Buffers are one code word deep only.

In the transmitter, insertion of SYNCD is determined by software control of the SYNCDC register.

In the receiver, locating a new packet by searching for the SYNCD pattern is controlled by the RDATAC command.

1: Transmit and receive buffers are two code words deep.

In the transmitter, insertion of SYNCD is automatic and depends on whether the code word is an address code word, determined by bit 0 of TXBUF0.

In the receiver, hardware determines the end boundary of the packet and automatically issues an RDATAC command when the packet is complete and the last code word is error free. The receiver continues to be responsive to software-generated RDATAC commands to force receiver D channel resynchronization.

Setting bit 6 High also redefines the DCHSTAT register bits to reflect the double buffer status.

Bits 5–0: Reserved

3.8.4 RXTMGR

Full name:Receive Timing Recovery RegisterAddress:FFC8Default:000x x000Access:read/write

RXTMGR enables timing recovery, specifies the timing recovery speed, and reports link synchronization status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC STATUS	PLL SPEED	SYNC RELEASE	reserved	reserved	MULTI- SAMPLE	RECOVERY SPEED	RX TIMING RECOVERY
	STATUS	STATUS				CONTROL	ENABLE

Bit 7: Synchronization Status (read only)

- 0: The receiver has not acquired frame synchronization.
- 1: The receiver has acquired frame synchronization. This condition is always true for a CFP that has begun transmission.

Bit 6: Phase-Locked Loop Speed Status (read only)

- 0: The receiver phase-locked loop may be in high-speed or low-speed mode, according to the value programmed in bit 1.
- 1: The receiver has detected a SYN channel marker; therefore, the PLL response is automatically forced to low speed, regardless of bit 1.

Bit 5: Synchronization Release Status (read only)

- 0: Default. A zero also indicates that frame synchronization is cleared because of a write to SYNCTR.
- 1: SYNCTR has been written to initiate clearing the frame synchronization, but it is not yet cleared.
- Bits 4–3: Reserved
- Bit 2: Receiver Multisampling

When disabled, the receiver samples data once in the middle of the bit period. When enabled, receive data is calculated as the value occurring at least twice among three samples, taken symmetrically about the center of the bit period and separated by 1.7 μ s. Multiple sampling functions only when timing recovery is enabled in bit 0; if bit 0 is cleared, the receiver samples singly, regardless of bit 2.

- 0: Single receive sampling
- 1: Multiple receive sampling
- Bit 1: Phase-Locked Loop Timing Recovery Speed Control
 - 0: High-speed response, changing to low speed automatically
 - 1: Forced low-speed response

Bit 0: Receiver Timing Recovery Enable When set, this control enables the clock recovery PLL and allows it to adjust the receive data sampling window.

- 0: Disable
- 1: Enable

3.8.5 **TXMUX**

Full name:Transmit Frame Control RegisterAddress:FFC9Default:xxxx x011Access:read/write

TXMUX controls the multiplex mode of the transmitter and selects the SYNC or CHM pattern for the SYN channel.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	TX SYN SELECT	TX N	MUX

Bits 7–3: Reserved

Bit 2: Transmit SYN Channel Pattern Select

0: CHMP or CHMF, depending on the DEVMODE register

1: SYNCF or SYNCP, depending on the DEVMODE register

Bits 1–0: Transmit Multiplex Selection

The formatter is cleared if TXMUX and RXMUX are both programmed for MUX3.

- 00: MUX1.2
- 01: MUX1.4
- 10: MUX2
- 11: MUX3

3.8.6 **RXMUX**

Full name:Receive Frame Control RegisterAddress:FFCADefault:xxxx 0011Access:read/write

RXMUX controls the multiplex mode of the receiver and selects the SYNC or CHM pattern for the receive SYN channel.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	SYNTOL	RX SYN SELECT	RX	MUX

Bits 7–4: Reserved

Bit 3: SYN Channel Error Tolerance Enable

- 0: Accept a SYN channel pattern only if all 24 bits are correct.
- 1: Accept a SYN channel pattern if at least 23 of 24 bits are correct. The error tolerance function is intended to improve initial frame timing recovery in noisy or intermittent transmissions. No SYN channel error will be reported if the pattern is accepted.

Bit 2: Receive SYN Channel Pattern Select

- 0: CHMP or CHMF, depending on the DEVMODE register
- 1: SYNCF or SYNCP, depending on the DEVMODE register

Bits 1–0: Receive Multiplex Selection

The formatter is cleared if RXMUX and TXMUX are both programmed for MUX3.

- 00: MUX1.2
- 01: MUX1.4
- 10: MUX2
- 11: MUX3

3.8.7 TXDISAB

Full name: Address: Default: Access: Transmit Disable Register FFCB <u>xxxx xx</u>01 write only

TXDISAB aborts a transmission or disables the transmitter but does not clear frame synchronization.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	ΤX	ТХ
						ABORT	DISABLE

Bits 7-2: Reserved

Bit 1: Transmit Abort

- 0: Default (transmission not aborted)
- 1: Immediately stop transmission at the end of the current frame, regardless of bit 0.

Note: Writing 03H also causes an immediate disable and 00H restarts transmission.

Bit 0: Transmit Disable

Transmission will start when data is loaded in the transmit buffer and this bit is cleared. Setting this bit disables the transmission at the end of the current transmit code word if data is still present in the transmit buffer. If the transmit buffer is empty, transmission stops at the end of the current frame. If the bit is set and then cleared prior to the end of a transmission, the write is ignored and transmission is not terminated.

- 0: Enable transmission
- 1: Disable transmission at the end of the code word

3.8.8 **SYNCDC**

Full name: Address: Default: Access: SYNCD Control Register FFCC <u>xxxx xxx</u>0 read/write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	SYNCD CONTROL						

Bits 7–1: Reserved

Bit 0: SYNCD Control

SYNCDC controls insertion of the D channel SYNCD pattern. The control bit is ignored if double buffering is enabled in DEVMODE[6].

- 0: The SYNCD pattern is not inserted prior to the next code word transmission.
- 1: The SYNCD pattern is inserted in the D channel before the next transmit code word, indicating the beginning of a new packet.

3.8.9 RDATAC

Full name:	Receive D Channel Data Control Register
Address:	FFCD
Default:	not applicable
Access:	write only

RDATAC is a command (address decode) with no associated data field that locates the beginning of the next receive D Channel packet by seeking the SYNCD pattern. Once software writes RDATAC, all D channel data is ignored by hardware until the SYNCD pattern is received, then the D channel code word will be loaded into the receive buffer RXBUF0–5.

The software must issue the RDATAC command to initiate D channel reception. The software must also issue the RDATAC command to locate the beginning of each new D channel packet. If double buffering is enabled, RDATAC is issued automatically by hardware if the packet is received without error. Under error conditions, software is responsible for issuing the command. If single buffering is used, software is always responsible for determining whether to issue RDATAC after each received code word.

3.8.10 **TPOWER**

Full name: Address: Default: Access: Transmit Power Control Register FFCE 00<u>xx xxx</u>0 read/write

TPOWER controls the TXPWR and CLK4M pins.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXP MO	WR DE	reserved	reserved	reserved	reserved	reserved	CLK4M ENABLE

Bits 7–6: TXPWR Pin Mode Selection

- 00: TXPWR goes High and stays High after the transmit portion of the current CT2 frame.
- 01: TXPWR is High during the transmit portion of the frame and Low during the receive portion, with timing the same as that of the TXEN pin.
- 1x: TXPWR goes Low and stays Low after the end of the transmit portion of the current CT2 frame.
- Bits 5–1: Reserved
- Bit 0: CLK4M Enable
 - 0: The 4.608-MHz CLK4M signal is disabled and held Low.
 - 1: The CLK4M signal is enabled on the CLK4M pin.

3.8.11 **BVALID**

Full name: Address: Default: Access: B Channel Valid Register FFCF 0<u>xxx xxxx</u> read/write

BVALID enables the CT2 B channel.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B CH	reserved						
ON/OFF							

Bit 7: B Channel On/Off

- 0: Transmit and receive paths between the CT2 B channel and the 32-kbps ADPCM data stream at the B Channel Multiplexer are disabled. The B Channel Multiplexer output goes to zero in both the transmit (to CT2 link) and receive (from CT2 link) directions.
- Transmit and receive CT2 B channel paths are enabled; that is, the CT2 B channel is connected to the 32-kbps ADPCM stream of the B Channel Multiplexer. There is a restriction that MECTR1[4] be enabled at least 1.25 ms before this bit is asserted to guarantee that embedded FIFO storage is appropriately loaded for operation.

Bits 6–0: Reserved

3.8.12 SYNCTR

Full name:	Frame Sync Control Command
Address:	FFD0
Default:	not applicable
Access:	write only

SYNCTR is a command (address decode) with no associated data field. Writing SYNCTR causes the frame synchronization to be cleared.

If synchronization has not been achieved, writing SYNCTR immediately clears any state machines attempting to synchronize to the SYN channel.

If synchronization has already been achieved, it will be cleared at the end of the transmit portion of the current CT2 frame, approximately 14 μ s before the next rising edge of the RXEN pin.

Note: When resynchronizing during a transmission, TXDISAB must be written before SYNCTR in order to disable transmission cleanly. Otherwise, unexpected transmit frame timing may result.

3.8.13 **DMONIT**

Full name:D Channel Monitor Control RegisterAddress:FFD1Default:xxxx xx00Access:read/write

DMONIT defines the CT2 test mode configuration applicable when the BDMUX register is programmed for D channel input/output (BDMUX[6:5]=10).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	TX D CH I/O MODE	MONITOR MODE

Bits 7–2: Reserved

Bit 1: Tx D Channel Data I/O Selection

- 0: The DTXDATAIO signal on the BDP1_OUT3 multifunction pin is an output and is a copy of what is being transmitted on the CT2 link.
- 1: The DTXDATAIO signal on the BDP1_OUT3 multifunction pin is an input, which will be transmitted on the CT2 link.

Bit 0: Monitor Mode

- 0: The DTXDATAIO signal on BDP1_OUT3 includes only D channel data. The DCT2RX signal on BDP0_OUT2 is an output that includes only D channel data.
- 1: The DTXDATAIO signal includes D channel, B channel, and SYN channel (except for preamble) data. The DCT2RX signal is an output that includes D, B, and SYN channel data (except for preamble).

3.8.14 DTXCTR

Full name:D Channel Transmit Control RegisterAddress:FFD2Default:xxxx xx00Access:read/write

DTXCTR specifies when the D channel transmit buffer empty interrupt is generated as well as specifying a continuous D channel transmit mode.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	ТХ	CONTIN
						BUFFER	ТХ
						EMPTY	
						CONTROL	

Bits 7–2: Reserved

- Bit 1: D Channel Transmit Buffer Empty Interrupt Control
 - 0: The transmit buffer empty (or half-empty) interrupt is generated when the last byte of the code word is loaded from the buffer into a serializing shift register.
 - 1: The transmit buffer empty interrupt is generated when the last bit of the code word (i.e., the parity bit) is transmitted.

Bit 0: D Channel Continuous Transmit Mode Select

- 0: Normal mode. After the transmit buffer is empty, D channel bits are filled with the IDLE_D pattern until the next code word is initiated. Emptying the buffer causes the transmit buffer empty interrupt.
- 1: Continuous transmission mode. Code words including the same six bytes of the transmit buffer are transmitted repeatedly. The transmit buffer empty interrupt is not generated. If the transmit MUX is set to 1.2, 1.4, or 2, then the 48-bit IDLE_D pattern is also transmitted between code words.
3.8.15 **BSYNC**

Full name:Burst Synchronization ControlAddress:FFD3Default:0000 0000Access:read/write

BSYNC controls synchronization to the 500-Hz CT2 frame synchronization signal in order to comply with Annex N of I-ETS 300 131. BSYNC must be configured before the CT2 Formatter is brought out of its cleared state (TXMUX[1:0]=RXMUX[1:0]=11).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ENSYNC	S/M	EDGE		E	BURST DEL	AY	

Bit 7: Enable 500-Hz Synchronization

- 0: Disabled. The CT2 Formatter is not synchronized to the 500-Hz SYNC.
- Synchronize Formatter to 500-Hz SYNC. Applies to CFP only. MECTR1[4] must be set to generate the 500-Hz signal as either a master or a slave.
- Bit 6: 500-Hz Slave/Master. Applies only if bit 7 is set.

Important Note: The Am79C411 must be configured as a slave if bit 7 is set.

- 0: Master.
- 1: Slave. The CT2 Formatter synchronizes to an internal 500-Hz clock phase-locked to the SYNC input at P1.6. P1SRC2[6] must be set High.

Bit 5: 500-Hz SYNC Edge

- 0: Rising-edge alignment
- 1: Falling-edge alignment
- Bits 4–0: Burst Sync Delay

Five bits specify the receive demodulator RF delay T_{RXRF} shown in Figure 2-8, which is used with the Modem Delay Register to determine the baseband data timing relative to the location of the 500-Hz SYNC signal. The programmable range is 0 to 6.75 bits (0 to 94 μ s) in 1/4-bit intervals.

Bits 4–2	Bit Delay	Bits 1–0	Phase Delay
000	0 bits	00	0/4 bit
001	1 bit	01	3/4 bit
010	2 bits	10	2/4 bit
011	3 bits	11	1/4 bit
100	4 bits		
101	5 bits		
110	6 bits		

3.9 TDELAY

Full name: Address: Default: Access: Transmit RF Delay Control FFD4 1000 1011 read/write

TDELAY controls the timing of the TXEN RF control pin relative to data transmission. Refer to Figure 2-12 for definition of timing parameters.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TTD D	ELAY			TTL	DELAY	-

Bits 7–4	Delay	Bits 7–4	Delay
0000	32.1 μs	0101	14.8 μs
0001	28.6 µs	0110	11.3 μs
0010	25.2 μs	0111	7.8 μs
0011	21.7 μs	1000	4.3 μs
0100	18.2 μs	1001	0.87 μs

 $\begin{array}{lll} \mbox{Bits 3-0:} & \mbox{Programmed delay } t_{\mbox{TTL}}. \ 4.3 \ \mu s \leq t_{\mbox{TTL}} \leq 46 \ \mu s \ in \ 3.47 \ \mu s \ increments. \\ & \mbox{Default} = 42.5 \ \mu s. \ \ Unspecified \ codes \ are \ invalid. \end{array}$

Bits 3–0	Delay	Bits 3–0	Delay
0000	4.3 μs	0111	28.6 µs
0001	7.8 μs	1000	32.1 μs
0010	11.3 μs	1001	35.6 μs
0011	14.8 μs	1010	39.0 µs
0100	18.2 μs	1011	42.5 μs
0101	21.7 μs	1100	46.0 μs
0110	25.2 μs		

3.9.1 RDELAY

Full name:Receive RF Timing ControlAddress:FFD5Default:<u>x</u>000 1011Access:read/write

RDELAY controls the timing of the RXEN RF control pin relative to data reception and configures the XINT2 pin to provide the ANTSW output timing signal. Refer to Figure 2-12 for definition of timing parameters.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	XINT2_ANTSW	FORCE		٦ ٦	RH DELA	Ý	
	SEL	RXEN					

Bit 7: Reserved

Bit 6: XINT2/ANTSW Select

- 0: XINT2_ANTSW pin performs XINT2 (external interrupt 2) input function.
- 1: XINT2_ANTSW pin performs ANTSW (antenna switch) output function.
- Bit 5: Force RXEN pin High, regardless of activity state of the CT2 Formatter. This feature allows receive level scanning without activating the CT2 Formatter.
 - 0: Default operation of RXEN.
 - 1: Force RXEN High.
- Bits 4–0: Programmed delay t_{TRH} . 11.3 μ s $\leq t_{TRH} \leq$ 87.6 μ s in 3.47 μ s increments. Default = 49.5 μ s. Unspecified codes are invalid.

Bits 4–0	Delay	Bits 4–0	Delay
00000	11.3 μs	01100	52.9 μs
00001	14.8 μs	01101	56.4 μs
00010	18.2 μs	01110	59.9 μs
00011	21.7 μs	01111	63.4 μs
00100	25.2 μs	10000	66.8 μs
00101	28.6 µs	10001	70.3 μs
00110	32.1 μs	10010	73.8 μs
00111	35.6 µs	10011	77.2 μs
01000	39.0 µs	10100	80.7 μs
01001	42.5 μs	10101	84.2 μs
01010	46.0 μs	10110	87.6 μs
01011	49.5 µs		

3.9.2 MODTMG

Full name:Modem Timing Adjustment RegisterAddress:FFDDDefault:xxxx xx00Access:read/write

MODTMG specifies whether delay is to be added to the transmit frame and initiates a delay measurement.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	reserved	NO	MEASURE
						DELAY	DELAY

Bits 7–2: Reserved

Bit 1: No Delay

- 0: The delay value in the MODDLY register determines the relative timing of the transmit and receive portions of the CT2 frame.
- 1: The transmit and receive portions of the CT2 frame are fixed as if the external RF delay were zero. That is, digital transmit and receive data signals at the chip meet the antenna timing constraints imposed by the CT2 CAI specification.

Bit 0: Delay Measurement Command Writing 1 initiates a modem delay measurement, which returns a value to the MODDLY register. Hardware clears the bit to indicate the end of the measurement. A software timer is recommended to time the measurement out in case of RF circuit failure.

- 0: No action (write); measurement complete (read).
- 1: Initiate measurement (write); measurement incomplete (read).

3.9.3 MODDLY

Full name:	Modem Delay Register
Address:	FFDE
Default:	<u>x</u> 000 0000
Access:	read/write

MODDLY reports the measured delay (read) and programs the desired delay (write). The total delay value, in 72-kHz bit periods, is

Total Delay = BIT DELAY + 1/16 · PHASE DELAY

The measured data can be read anytime after MEASURE DELAY (MODTMG[0]) is cleared after completion of a measurement, even after writing new values to this register. Reading the register always returns the measured value. Written values cannot be read. If MEASURE DELAY has never been set, the default value is returned.

Writes to this register should not take place while the MEASURE DELAY bit is set.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved		PH	ASE		BIT		
		DE	LAY			DELAY	

Bit 7: Reserved

Bits 6–3: Phase Delay These bits report in binary form the measured phase delay when read and specify the desired phase delay when written. Each phase increment is 1/16th of 1 bit or 868 ns.

Bits 2–0: Bit Delay These bits report in binary form the measured bit delay when read and specify the desired bit delay when written. Each increment represents a delay of 1 bit or 13.89 μs.

Note: The maximum modern delay value is $6\frac{15}{16}$ bits, or 96 μ s.

3.9.4 DCHSTAT

Full name:D Channel Status RegisterAddress:FFE4Default:<u>0</u>000 0100Access:read only

DCHSTAT reports the CT2 D channel transceiver status. DCHSTAT bits have no individual mask bits, but appear in MISRC0[2:0] subject to mask bits MIMSK0[2:0].

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	reserved	DTX FMPTY	DRX ERR	DRX FULL
TESEIVEU	reserveu	reserveu	reserveu	TESEIVEU	EMPTY	ERR	F

The following definitions apply when DEVMODE[6]=0, Single Buffering

- Bits 7–3: Reserved. Reads return zeroes, subject to change in future silicon revisions.
- Bit 2: D Channel Transmit Buffer Empty Note that the DTX EMPTY interrupt **defaults to ACTIVE** and that it remains active until the buffer is filled. Therefore, software should mask the interrupt until after the buffer is written. This bit is cleared by writing to the transmit buffer, TXBUF0–TXBUF5.
 - 0: The CT2 D channel transmit buffer TXBUF is not empty.
 - 1: TXBUF is empty (default). Empty is defined by the DTXCTR register, bit 1.

Bit 1: D Channel Receive CRC, Parity Error, or Overflow

- This bit is cleared when the DCHSTAT register is read.
- 0: There is no CRC, parity, or overflow error.
- 1: A CRC, parity, or overflow error occurred in the D channel receiver.
- Bit 0: D Channel Receive Buffer Full
 - This bit is set when the buffer is full and cleared when RXBUF5 is read.
 - 0: The receive buffer has not been filled since RXBUF5 was last read.
 - 1: The D channel receive buffer, RXBUF0–RXBUF5, contains 6 bytes.

The following definitions apply when DEVMODE[6]=1, Double Buffering

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	DRX OVF	DTX UF	DTX HALF EMPTY	DRX FULL	DTX EMPTY	DRX ERR	DRX HALF FULL

Bit 7: Reserved. Reads return zeroes, subject to change in future silicon revisions.

- Bit 6: RX Overflow Status Read only. Active High if the D Channel Receive Buffer has overflowed, indicating possible erroneous buffer contents. This bit should be evaluated each time the receive buffer is read to validate buffer contents.
 - 0: No overflow (default)
 - 1: Overflow

Bit 5: TX Underflow Read only. Active High if the D Channel Transmit Buffer has underflowed,

indicating that the D channel may have been stuffed with IDLE_D bits. Cleared by reading the register. This bit should be evaluated each time the transmit buffer is loaded to validate the contents of the actual transmitted D channel stream.

- 0: No underflow (default)
- 1: Underflow
- Bit 4: TX Buffer Half-Empty

Read only. Active High if the D Channel Transmit Buffer contains one code word or less, indicating that software should load another code word into the D channel buffer. Cleared when software loads the buffer.

- 0: Buffer contains two code words.
- 1: Transmit buffer is half full (i.e., contains one code word or less) (default).

Bit 3: RX Buffer Full

Read only. Active High if the D Channel Receive Buffer contains two code words (12 bytes), indicating that software should read a code word from the D channel buffer to avoid overflow. Cleared when software reads a code word from the buffer.

- 0: Buffer does not contain two code words (default).
- 1: Buffer is full (i.e., contains two code words).
- Bit 2: TX Buffer Empty

Read only. Active High if the D Channel Transmit Buffer contains no code words, indicating that software should load another code word into the D channel buffer to avoid underflow. Note that the DTX EMPTY interrupt **defaults to ACTIVE** and that it remains active until the buffer is loaded. Therefore, software should mask the interrupt until after the buffer is written. Cleared when software loads the buffer.

- 0: Buffer contains at least one code word.
- 1: Buffer is empty (i.e., contains no data) (default).
- Bit 1: RX Error

Read only. Active High if the D Channel Receive Buffer code word accessible by software contains a CRC or Parity error. This bit should be evaluated before the actual contents of the buffer are read because the act of reading one part of the double buffer switches the software access to the second part.

- 0: No parity or CRC error is detected in the accessible code word (default).
- 1: Accessible code word in the receive buffer contains a parity or CRC error.
- Bit 0: RX Buffer Half Full

Read only. Active High if the D Channel Receive Buffer contains at least one code word (6 bytes), indicating that software should read a code word from the D channel buffer. Cleared when software reads a code word from the buffer.

- 0: Buffer contains less than one code word (default).
- 1: Buffer is half full (i.e., contains at least one code word).

3.9.5 CMSSRC

Full name:CHM/SYNC Interrupt Source RegisterAddress:FFE5Default:xxxx 0000Access:read only

CMSSRC reports CT2 SYN channel interrupt sources. Bits are latched to 1 only when an interrupt event occurs while the associated mask bit in CMSMASK is set. All bits are cleared by reading the register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	SYNC	SYNCD	SYNC	CHM
				ERR			

Bits 7–4: Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 3: The SYNC ERROR interrupt occurs if the appropriate SYN channel pattern (SYNCF, SYNCP, CHMF, or CHMP), as determined by the DEVMODE and RXMUX registers, is not received at the expected time during a CT2 reception.

- 0: There has been no synchronization error or CMSMASK[3]=0.
- 1: The SYN channel pattern was not received correctly and CMSMASK[3]=1.
- Bit 2: The SYNCD interrupt occurs when a SYNCD pattern is received in the D channel.
 - 0: No SYNCD has been received or CMSMASK[2]=0.
 - 1: A SYNCD pattern has been received and CMSMASK[2]=1.
- Bit 1: The SYNC interrupt occurs when the SYN channel receiver correctly receives either a SYNCF or a SYNCP pattern, depending on whether the device is programmed as a CFP or a CPP in the DEVMODE register.
 - 0: No SYNC has been received or CMSMASK[1]=0.
 - 1: A SYNC pattern has been received and CMSMASK[1]=1.
- Bit 0: The CHM interrupt occurs when the SYN channel receiver correctly receives either a CHMF or a CHMP pattern, depending on whether the device is programmed as a CFP or a CPP in the DEVMODE register.
 - 0: No CHM has been received or CMSMASK[0]=0.
 - 1: A CHM pattern has been received and CMSMASK[0]=1.

3.9.6 CMSMASK

Full name:CHM/SYNC Mask RegisterAddress:FFE6Default:xxxx 0000Access:read/write

CMSMASK provides individual enables for each interrupt source in CMSSRC.

0: Disable interrupt

1: Enable interrupt

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	reserved	reserved	SYNC ERR	SYNCD	SYNC	CHM

Bits 7–4 Reserved

Bit 3: SYNC Error Interrupt Mask

Bit 2: SYNCD Interrupt Mask

Bit 1: SYNC Interrupt Mask

Bit 0: Channel Marker Interrupt Mask

3.10 INTERRUPT CONTROLLER

3.10.1 MISRC0

Full name:	Main Interrupt Source Register 0
Address:	FFE0
Default:	<u>00</u> 00 0000
Access:	read only

A 1 in any bit of MISRC0 causes an active (Low) level at the 8032 INT0 input. Bits are individually enabled in MIMSK0.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	JITTER	EXTINT2	EXTINT1	DTX	DRX	DRX
					EMPTY	ERR	FULL

Bits 7–6: Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 5: JITTER

The jitter interrupt indicates that the jitter detector has detected jitter in the CT2 link in excess of the threshold programmed in the JITCTR register or that the DSP-based noise detector has triggered. This bit reports the logical OR of the jitter status NSCTR[7], subject to the mask bit MIMSK0[5], and the noise status NSCTR[6], subject to its mask NSCTR[5]. NSCTR[7] is cleared by reading NSCTR.

- 0: The jitter interrupt or DSP-based noise detector is inactive or MIMSK0[5] =0.
- 1: The jitter interrupt is active and MIMSK0[5]=1 or DSP-based noise detector is active and NSCTR[5]=1.
- Bit 4: EXTINT2

External Interrupt 2 is generated by a change of state of the XINT2_ANTSW pin and is cleared by reading XISTAT2.

- 0: There is no EXTINT2 interrupt active or MIMSK0[4]=0.
- 1: The EXTINT2 interrupt is active and MIMSK0[4]=1.
- Bit 3: EXTINT1

External Interrupt 1 is generated by a change of state of the XINT1 pin and is cleared by reading XISTAT1.

- 0: There is no EXTINT1 interrupt active or MIMSK0[3]=0.
- 1: The EXTINT1 interrupt is active and MIMSK0[3]=1.
- Bit 2: DTXEMPTY is the D channel transmit buffer empty status, DCHSTAT[2], subject to MIMSK0[2].
 - 0: The D channel transmit buffer is full or MIMSK0[2]=0.
 - 1: The D channel transmit buffer is either empty or half-empty, as determined by DCHSTAT[4,2] and MIMSK0[2]=1. The half-empty status causes an interrupt only if double buffering is enabled in DEVMODE[6].
- Bit 1: DRX ERR is the D channel receive error status, DCHSTAT[1], subject to MIMSK0[1].
 - 0: No D channel receive parity, CRC, or overflow error has been detected or MIMSK0[1]=0.
 - 1: A D channel receive error has been detected and MIMSK0[1]=1.

- Bit 0: DRXFULL is the D channel receive buffer full status, DCHSTAT[0], subject to MIMSK0[0].
 - 0: The D channel receive buffer, RXBUF0–RXBUF5, does not contain a complete code word or MIMSK0[0]=0.
 - 1: RXBUF contains either one or two complete code words, as determined by DCHSTAT[3,1], and MIMSK0[0]=1. The receive buffer can contain two code words only if double buffering is enabled in DEVMODE[6].

3.10.2 MISRC1

Full name:Main Interrupt Source Register 1Address:FFE1Default:<u>0</u>000 0000Access:read only

A 1 in any bit of MISRC1 causes an active (Low) level at the 8032 INT1 input. Bits are individually masked in MIMSK1.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	P1 INT 2	P1 INT 1	P1 INT 0	CHM/ SYNC	SIO	reserved	EXTINT0

Bit 7: Reserved. Reads return zeroes, subject to change in future silicon revisions.

Bit 6: P1 INT 2

Port 1 Interrupt 2 is active when an interrupt at pins P1.7–P1.4 has occurred, enabled by P1MASK, and is cleared by reading P1SRC2.

- 0: No interrupts on pins P1.7–P1.4 have occurred or MIMSK1[6]=0.
- 1: An interrupt on pins P1.7–P1.4 has occurred and MIMSK1[6]=1.
- Bit 5: P1 INT 1

Port 1 Interrupt 1 is active when an interrupt at pins P1.3 or P1.2 has occurred, enabled by P1MASK, and is cleared by reading P1SRC1.

- 0: No interrupts on pins P1.3 or P1.2 have occurred or MIMSK1[5]=0.
- 1: An interrupt on pins P1.3 or P1.2 has occurred and MIMSK1[5]=1.
- Bit 4: P1 INT 0

Port 1 Interrupt 0 is active when an interrupt at pins P1.1 or P1.0 has occurred, enabled by P1MASK, and is cleared by reading P1SRC0.

- 0: No interrupts on pins P1.1 or P1.0 have occurred or MIMSK1[4]=0.
- 1: An interrupt on pins P1.1 or P1.0 has occurred and MIMSK1[4]=1.
- Bit 3: CHM/SYNC

The channel marker/SYNC interrupt is active if any of the four interrupt sources reported in CMSSRC is true, subject to MIMSK1[3], and is cleared by reading CMSSRC.

- 0: No CMSSRC bit is set or MIMSK1[3]=0.
- 1: A CMSSRC bit is set and MIMSK1[3]=1.
- Bit 2: SIO

The serial port interrupt is active when either of the two interrupt sources reported in SIOSRC are true, and is cleared when SIOSRC is read.

- 0: There is no serial port interrupt or MIMSK1[2]=0.
- 1: There is a serial port interrupt and MIMSK1[2]=1.
- Bit 1: Reserved. Reads return zeroes, subject to change in future silicon revisions.
- Bit 0: EXTINT0 External Interrupt 0 is generated by a change of state of the XINT0 pin and is cleared by reading XISTAT0.
 - 0: There is no EXTINT0 interrupt active or MIMSK1[0]=0.
 - 1: The EXTINT0 interrupt is active and MIMSK1[0]=1.

3.10.3 MIMSK0

Full name:Main Interrupt Mask Register 0Address:FFE2Default:0000 0000Access:read/write

MIMSK0 provides individual enables for each interrupt source in MISRC0.

- 0: Disable interrupt
- 1: Enable interrupt

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	JITTER	EXTINT2	EXTINT1	DTX	DRX	DRX
					EMPTY	ERR	FULL

Bits 7–6: Reserved, unused. Reads return zeroes, subject to change in future silicon revisions.

- Bit 5: Jitter Interrupt Mask
- Bit 4: External Interrupt 2 Mask
- Bit 3: External Interrupt 1 Mask
- Bit 2: D Channel Transmit Buffer Empty Interrupt Mask
- Bit 1: D Channel Receive Error Interrupt Mask
- Bit 0: D Channel Receive Buffer Full Interrupt Mask

3.10.4 **MIMSK1**

Full name:	Main Interrupt Mask Register 1
Address:	FFE3
Default:	<u>0</u> 000 00 <u>0</u> 0
Access:	read/write

MIMSK1 provides individual enables for each interrupt source in MISRC1.

- 0: Disable interrupt
- 1: Enable interrupt

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	P1 INT 2	P1 INT 1	P1 INT 0	CHM/ SYNC	SIO	reserved	EXTINT0

Bit 7: Reserved, unused. Reads return zeroes, subject to change in future silicon revisions.

- Bit 6: Port 1 Interrupt 2 Mask
- Bit 5: Port 1 Interrupt 1 Mask
- Bit 4: Port 1 Interrupt 0 Mask
- Bit 3: CHM/SYNC Interrupt Mask
- Bit 2: Serial Port Interrupt Mask
- Bit 1: Reserved, unused. Reads return zeroes, subject to change in future silicon revisions.
- Bit 0: External Interrupt 0 Mask

3.11 CLOCK GENERATOR (POWER MANAGEMENT)

3.11.1 UCCCTR

Full name:	Shutdown/Microcontroller Clock Control register
Address:	FFE9
Default:	00 <u>xx x</u> 000
Access:	read/write

UCCCTR controls the low-power shutdown mode and the 8032 clock rate. Write access to UCCCTR is restricted by the UCCCP address decode protection mechanism, but UCCCTR read access is unrestricted.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SHUT	AUTO	reserved	reserved	reserved	C	PU CLK RAT	ГЕ
	SPEED						
	UP						

Bit 7: Setting the SHUTDOWN bit starts a timer which places the chip in shutdown mode in 3.56 ms (min) to 7.12 ms (max). Any unmasked interrupt (INT0 or INT1) aborts the sequence and clears the bit. The bit is automatically cleared when the device exits shutdown.

- 0: Disable shutdown sequence or halt shutdown sequence.
- 1: Initiate shutdown sequence if none running, or restart the sequence if already running.

Bit 6: Setting the CPU clock automatic speedup mode allows the CPU clock generator to increase the CPU clock rate to 9.216 MHz when any unmasked interrupt (INT0 or INT1) occurs.

- 0: Disable auto speedup
- 1: Enable auto speedup
- Bits 5–3 Reserved
- Bits 2–0: CPU CLK RATE determines the rate of the 8032 clock, CPUCLK, which may be configured as an output on the CS2_CPUCLK pin. Table 3-8 lists codes for CPUCLK rate. The bits are cleared by software or by the automatic speed-up mechanism.

Table 3-8 8032 CPUCLK Speed Codes

CPU CLK RATE	CPUCLK
210	Rate
000	9.216 MHz
001	4.608 MHz
010	2.304 MHz
011	1.152 MHz
100	576 kHz
101	288 kHz
110	144 kHz
111	72 kHz

3.11.2 UCCCP

Full name:	Shutdown/Microcontroller Clock Control Protection
Address:	FFEA
Default:	not applicable
Access:	write only

This write-only address decode is part of the mechanism to protect the shutdown/microcontroller clock control register (UCCCTR) against inadvertent writes. There is no data field associated with the UCCCP address.

Software must perform the following sequence of events consecutively without interruption to change the contents of UCCCTR.

- 1. Write arbitrary data to UCCCP.
- 2. Write arbitrary data to UCCCTR.
- 3. Write arbitrary data to UCCCP.
- 4. Write desired immediate data to UCCCTR.

If any other reads or writes occur during the sequence, the sequence is aborted. This implies that all loading of the UCCCTR must be done with data stored either as immediate data in program space or else stored in 8032 internal data space (e.g., auxiliary registers, internal 256 byte RAM, etc.).

3.11.3 MECTR0

Module Enable Control Register 0
FFEB
<u>x0x</u> 0 <u>xx</u> 00
read/write

MECTR0 enables specific functions within the chip for power management reasons. Each enable bit is gated with the shutdown mode indicator so that all blocks are automatically disabled when the chip is in shutdown and restored to their programmed state after the chip wakes up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	ADPCM	reserved	SIO	reserved	reserved	T0/T1	T0/T1
	ENABLE		ENABLE			ENABLE	FORCE

Bit 7: Reserved

- Bit 6: ADPCM Transcoder and Dual-Tone Generator enable
 - 0: Disable
 - 1: Enable. MECTR1[4] must also be enabled to provide frame timing.
- Bit 5: Reserved
- Bit 4: Serial port enable
 - 0: Disable
 - 1: Enable the synchronous serial port block using the SDIN, SDOUT, and SCLK pins.
- Bits 3–2: Reserved
- Bit 1: 8032 Timer/counter 1 and 0 clock enables. 8032 T0 and T1 signals (P3.5 and P3.4) are internally connected to a common 18-kHz clock, enabled by this bit.
 - 0: Disable; T0 and T1 signals are held at a level determined by MECTR0[0].
 - 1: Enable
- Bit 0: T0/T1 FORCE, applicable only when MECTR0[1]=0.
 - 0: 8032 T0 and T1 signals are held High.
 - 1: 8032 T0 and T1 signals are held Low.

3.11.4 MECTR1

Module Enable Control Register 1
FFEC
<u>xx</u> 00 00 <u>x</u> 0
read/write

MECTR1 enables specific functions within the chip for power management reasons. Each enable bit is gated with the shutdown mode indicator so that all blocks are automatically disabled when the chip is in shutdown and restored to their programmed state after the chip wakes up.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
reserved	reserved	TX	B CH	FORMAT	FORMAT	reserved	RSSI
		MOD	MUX/	ENABLE	ENABLE		ENABLE
		ENABLE	FRAME SYNC	1	2		
			ENABLE				

Bits 7–6: Reserved

- Bit 5: Transmit Modulator Enable
 - 0: Disable
 - 1: Enable
- Bit 4: B Channel Multiplexer and Frame Sync Enable
 - 0: Disable the B Channel Multiplexer, the 8-kHz PCM frame sync which times the 32-kbps B channel port, and the 500-Hz CT2 frame synchronization clock.
 - 1: Enable the B Channel Multiplexer and the 8-kHz PCM frame sync, CLK8K. Also enable internal generation of a 500-Hz clock for CT2 link synchronization.
- Bits 3–2: CT2 Formatter Enables 1 and 2
 - 00: Disable the CT2 Formatter
 - 11: Enable basic CT2 Formatter. Both bits must be set High to enable the formatter.
- Bit 1: Reserved
- Bit 0: RSSI Enable
 - 0: Disable
 - 1: Enable. Allow 300 μ s for settling after the RSSI is enabled.

3.11.5 WDTKEY

Full name:	Watchdog Timer Key Register
Address:	FFEF
Default:	not applicable
Access:	write only

WDTKEY must be accessed in a certain sequence at least once every 1.82 seconds, or the watchdog timer will generate a reset pulse, returning the chip to its default state. The key sequence is:

> write WDTKEY = A5 hex write WDTKEY = 5A hex

The sequence must be written without interruption in consecutive write cycles.

Do not write the key sequence within the first 120 ms after reset is released. Timing information drawn from the watchdog timer after reset initializes some analog circuits, and writing the key sequence during this period may interrupt this initialization.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
WDTKEY								

SOFTWARE APPLICATIONS

5.1 SHUTDOWN MODE

Shutdown mode disables all synchronous and analog circuits in order to minimize power consumption.

Necessary software actions are:

- 1. Set the shutdown mode by programming UCCCTR[7] to 1.
- 2. Program PCFIG to #01H and P3PCRB to #060H to disable weak pull-ups on ports P3.4 and P3.5 for minimal power consumption. PCFIG and P3PCRB are 8032 special function registers (SFR) unique to the PhoX chip. Do not disable other 8032 weak pull-ups because other port pins may float and actually increase power consumption.
- 3. Place the microcontroller in idle mode by programming PCON[0] to 1 within 3.56 ms of programming UCCCTR[7].

Some optional actions may make system behavior more predictable. The following optional operations should be done either before setting the shutdown mode bit or between setting the shutdown bit and programming the microcontroller for idle mode.

- Disable all blocks by clearing the registers MECTR0 and MECTR1.
- Program the microcontroller auto speed-up feature in UCCCTR[6].
- Program the main interrupt masks, MIMSK0 and MIMSK1.
- Service the watchdog timer.

Any unmasked interrupt causes the chip to awaken from shutdown mode and the microcontroller to exit idle mode.

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5.2 CT2 FORMATTER PROGRAMMING HINTS

Steps in programming the formatter:

1. Enable the CT2 Formatter in MECTR1.	MECTR1[3:2]=11
2. Program for CFP or CPP.	DEVMODE
3. If the device is a CPP, enable timing recovery.	RXTMG = 0x01
4. Program the modem delay, if applicable.	
5. Release receiver synchronization.	Write SYNCTR command
6. Disable transmitter.	TXDISAB = 0x01
7. Set the SYNCD pattern.	SYNCDC = 0x01
8. Ignore D channel receive until SYNCD is received.	Write RDATAC command
9. Disable B channel.	BVALID = 0x00
10. Program other CT2 Formatter registers, as necessary	
11. Enable interrupts.	
12. Program transmission/reception multiplex.	TXMUX, RXMUX

SYNCDC Register

If using single buffering, always be sure to write the SYNCDC register to the desired state before loading the transmit buffer.

Transmitting MUX2 or MUX3

To transmit MUX2 or MUX3, the TXDISAB and SYNCTR addresses, if written, should be written after loading the TXBUF buffer; the other registers should be written before loading the transmit buffer registers.

5.3 TO AND T1 TIMER/COUNTERS

Bit 1 of MECTR0 enables the common 18-kHz signal that is routed to both the T0 and T1 inputs of the microcontroller. The timer/counter circuits in the 8032 must be programmed as event counters in order to recognize the 18-kHz signal. There are also limitations on how slow the 8032 clock rate can be before the event counters fail to correctly count T0 and T1 transitions. Clock rates below 576 kHz do not accurately count the T0 and T1 timer/counter input because the sampling rate is too Low.

Note that timer interrupts do not activate the PhoX controller auto speedup feature; therefore, the time to service the interrupt depends on the microcontroller clock speed.

5.4 P1 INTERRUPTS

Interrupts caused by transitions of the P1 port pins are grouped into three interrupt sources. In general, the P1 port is used for input and output. If the inputs and outputs are arranged such that only one P1 input exists per P1 interrupt source register (P1SRC0, P1SRC1, P1SRC2), then locating the cause of the interrupt is simplified because the P1 source register need not be examined.

It is possible to cause a false interrupt indication without the P1 input actually changing if the P1TRIG register is changed while the interrupt is unmasked. Therefore, the interrupt should be masked while the P1TRIG is written.

5.5 SERIAL PORT SERVICE

SIOWR and SIORD are service routines for writing to and reading from the EXEL Microelectronics 93C46 serial EEPROM. The example drives the 93C46 active-High chip select from port P1.1, which is arbitrarily chosen. The EEPROM device has a 16-bit data field and a 6-bit address field. It requires a start bit, an op-code, and a dummy bit during transmission. It has active-High clocks and read data should be sampled on the positive-going clock edge.

; Write to and read from the 93C46 Serial EEPROM device

acall INIT ; initialize the serial port registers

; Write the 16-bit value 0123 to address 1A.

setb	P1.1	;	set active high chip select
mov	R1, #03H	;;	R1 holds the transmit length argument, 3, in this example write
mov	R2, #05H	;;	R2 holds the data argument. 1 0 1 = start bit + 01 ("write" op code)
acall	SIOWR	; ;	send the start bit plus the two-bit write op-code
mov mov acall	R1, #06H R2, #1AH SIOWR	; ; ;	length = 6 bits address to be sent= 1AH = 01 1010 binary send the 6-bit address field, address = 1A.
mov mov acall	R1, #00H R2, #01H SIOWR	;;;	<pre>length = 8 bits data to be sent = 01H send the most significant data byte, data = 01</pre>
mov mov	R1, #00H R2, #23H	; ;	length = 8 bits data to be sent = 23H

acall SIOWR ; send the least significant data byte, data = 23 clr P1.1 ; clear the active high 93C46 chip select, finishing the write : ; Read back the value written to address 1A P1.1 ; set active high chip select setb mov R1, #03H; length = 3-bits R2, #06H; data to be sent is $1 \ 1 \ 0 =$ start bit + 10 ("read" mov op code) ; SIOWR ; send the start bit plus the two-bit read op-code acall mov R1, #06H; length = 6 bits R2, #1AH ; Load EEPROM address argument, 1AH mov acall SIOWR ; send the 6-bit address field, address = 1A, R1, #01H ; This device needs a "dummy" bit between transmit mov and receive, ; mov R2, #00H ; so send 1 bit (data is actually a don't-care). ; acall SIORD ; send the dummy bit and begin reception ; Data returned in DATA1 and DATA2 RAM ; locations clr P1.1 ; clear the active high 93C46 chip select and end the read loop 1 ; loop1: ajmp loopl ; infinite loop INIT: ; disabled the 93C46 chip select clr P1.1 DPTR, #MECTR0 mov A, @DPTR movx A, #10H orl movx A, @DPTR ; enable the serial port by asserting MECTR0[4] DPTR, #MIMSK1 mov movx A, @DPTR orl A, #04H @DPTR, A ; enable serial port interrupt by asserting movx MIMSK1[2] ; DPTR, #SPTMG mov A, #03H mov @DPTR, A ; set serial port clock rate to 288 kHz in SPTMG movx RET SIOWR: ; inputs: auxiliary register R1 = Transmit length ; R2 = Transmit data dptr, #SIOMODE mov A, #08H mov

```
@DPTR, A ; SIOMODE <- 08H. Mode = write only, active high
      movx
                          clocks
                      ;
             dptr, #SIOTBL
      mov
      mov
             A, R1
             @DPTR, A ; SIOTBL <- R1. Write transmit length register
     movx
             dptr, #SIOTB
      mov
             A, R2
     mov
             @DPTR, A ; SIOTB <- R2. Write transmit data
     movx
             dptr, #SIOMASK
      mov
             A, #02H
     mov
             @DPTR, A ; enable transmit buffer empty interrupt in
     movx
                          SIOMASK[1]
                      ;
      clr
             test.0
wait1:
      jnb
             test.0, wait1 ; wait until transmit buffer is empty
      RET
SIORD:
                                   R1 = Transmit length
;
   inputs: auxiliary register
;
                                   R2 = Transmit data
             dptr, #SIOMODE
     mov
             A, #0DH
     mov
     movx
             @DPTR, A ; mode = active high clock, + edge receive,
                      ; 16-bit receive length, write-then-read
      mov
             dptr, #SIOTBL
             A, R1
     mov
     movx
             @DPTR, A ; SIOTBL <- R1. Write transmit length register
             dptr, #SIOTB
     mov
             A, R2
     mov
             @DPTR, A ; SIOTB <- R2. Write transmit data
     movx
     mov
             dptr, #SIOMASK
             A, #01H
      mov
             @DPTR, A ; enable receive buffer full interrupt by setting
      movx
                          SIOMASK[0]
                      ;
             test.0
      clr
wait2:
      jnb
             test.0, wait2; wait until the receive buffer is full (1st byte)
      mov
             A, #TEMP
             #DATA1, A; store first received byte in RAM
      mov
             test.0
      clr
wait3:
      jnb
             test.0, wait3 ; wait until receive buffer is full (2nd byte)
      mov
             A, #TEMP
             #DATA2, A; store second received byte in RAM
      mov
      RET
```

```
ISR1:
; Interrupt Service Routine for \overline{\text{INT1}}, assuming serial port is the only
     interrupt source
;
     mov
           DPTR, #SIOSRC
           A, @DPTR
     movx
     rrc
           А
           TXINT
                   ; read SIOSRC to determine in interrupt is
     jnc
                   ; from the transmitter or the receiver
     mov
           DPTR, #SIORB
           A, @DPTR ; Read receive buffer. Leave data in accumulator.
     mov
     mov
           #TEMP, A ; temporary RAM storage of read data
TXINT:
           dptr, #SIOMASK
     mov
           A, #00H
     mov
           @DPTR, A ; clear interrupt mask
     movx
                  ; terminate the wait loop
     setb
           test.0
     RETI
                   ; return from interrupt
```



ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Storage temperature	.–65°C to +150°C
Ambient Temperature with power applied	40°C to +85°C
Supply voltage to ground potential, continuous	0 V to 6.0 V $$
Lead Temperature (10-s hot-bar soldering)	300°C
Lead Temperature (Reflow)	107°C
Maximum power dissipation	
Voltage from any pin to Vss: Vss-(0.3 V to Vcc+0.3 V
DC input/output fault current	30 mA

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

6.2 OPERATING RANGE

2.7 V to 3.60 V
2.7 V to 5.25V
. 0°C to +70°C
–20°C to +70°C
–40°C to +85°C

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

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6.3 DIGITAL I/O DC CHARACTERISTICS

Table 6-1 Digital Pin DC Characteristics

Over operating range, unless otherwise specified. (Applies to all pins except MXTAL1, MXTAL2, RSSI, TXI, TXQ, MREF, IREF, and CFILT)

Parameter	Parameter Description	Test Conditions	Min	Тур	Max	Unit
Cl	Pin input capacitance	temp = 25°C, freq = 1 MHz		10		pF
C _O	Pin output capacitance	temp = 25°C, freq = 1 MHz		15		pF
C _{L1}	Load capacitance (except TRI0_OUT10, TRI1)				40	pF
C _{L2}	Load capacitance, TRI0_OUT10, TRI1 pins				50	pF
lcc	Supply current	Vcc = 3 V, shutdown standby ⁽²⁾ active ⁽³⁾		0.036 4.0 12.5		mA
۱ _L	Input leakage, output high Z leakage	Vss < Vin < Vcc Vss < Vout (high Z) < Vcc			±10	μΑ
I _{OH}	Output current drive, driving 1	V_{OH} =2.4 V, Vcc=3 V ⁽¹⁾ V _{OH} = 2.6 V, Vcc = 3 V ⁽¹⁾	-2 -1			mA
I _{OL, 1}	Output current drive, driving 0. See note 4.	$V_{OL} = 0.4 V$, $Vcc = 3 V$ ⁽¹⁾ $V_{OL} = 0.7 V$, $Vcc = 3 V$ ⁽¹⁾	2 10			mA
I _{OL, 2}	Output current drive, driving 0. See note 5.	$V_{OL} = 0.4 V, Vcc = 3 V$	2			mA
R _{L1}	Resistance to Vss/Vcc for logic 0/1 (TRI0_OUT10, TRI1 pins)				50	Ω
R _{L2}	Leakage to Vss or Vcc for logical mid-supply (TRI0_OUT10, TRI1 pins)		250			kΩ
V _{IH}	Input High voltage	Vcc = 3 V	2.1		Vcc + 0.3	V
V _{IL}	Input Low voltage	Vcc = 3 V	-0.3		0.8	V
V _{OH}	Output High voltage (except reset)	$I_{OH} = -1 \text{ mA}, \text{ Vcc} = 3 \text{ V}$	2.4			V
V _{OL}	Output Low voltage	I _{OL} = 2 mA, Vcc = 3 V			0.4	V

Notes:

1. These parameters apply to all digital outputs when they are actively driven. Microcontroller port 1 and 3 pins are actively driven High for two cycles of the CPUCLK, and then held High by a weak "keeper" transistor.

- 2. Oscillator on, microcontroller clock = 576 kHz, CT2 Formatter, and RSSI A/D on; all other modules off.
- 3. I/Q modulator, CT2 Formatter, RSSI A/D modules on; microcontroller clock = 1.152 MHz, serial port on at 36-kHz clock rate.
- 4. I_{OL, 1} applies to the following pins: BDP0_OUT2 through BDP5_OUT11, <u>CS2</u>_CPUCLK, OUT6, OUT7, P1.7–P1.0, P3.7, P3.6, P3.1, P3.0, <u>PSEN</u>, SCLK, SDOUT, SHCTRL, TRI0_OUT10, TXPWR, XINT2_ANTSW.
- 5. I_{OL, 2} applies to the following pins: ALE, CLK4M, CS0_INT0, CS1_INT1, P0.7–P0.0, P2.7–P2.0, PCMCLK, PCMIN, PCMOUT, RE, RXEN, TE, TXEN.

6.4 AUDIO CHARACTERISTICS

6.4.1 ADPCM Transcoder Performance

The ADPCM transcoder is fully compliant with CCITT Recommendation G.721 for A-law and $\mu\text{-law}$ PCM input/output.

6.4.2 Dual-Tone Generator Performance

Appendix A lists frequency and amplitude error characteristics. DTMF signal to total distortion is 31-dB minimum, tested at the PCMOUT pin in A-law PCM format with 0-dB programmed gain.

6.5 RSSI CHARACTERISTICS

Table 6-2 applies to the RSSI pin. Inputs above the full scale V_{FS} read as full scale. Inputs below the minimum code input voltage V_{ZERO} read as the minimum input code.

Table 6-2 RSSI Characteristics

Parameter	Parameter Description	Test Conditions	Min	Тур	Max	Unit
ERR _{LIN}	RSSI A/D integral linearity error				±1	LSB
T _{CONV}	RSSI A/D conversion time			10		μs
V _{FS}	RSSI maximum code input voltage	Transition voltage between codes 11110 and 11111	1.188	1.250	1.313	V
V _{ZERO}	RSSI minimum code input voltage	Transition voltage between codes 00000 and 00001	0.236	0.244	0.248	V

6.6 I/Q MODULATOR CHARACTERISTICS

All spectral characteristics, Table 6-3, apply to TXI and TXQ outputs referenced to MREF and filtered by single pole passive low pass filters with 3-dB frequency of 100 kHz. All dBV values are based on the assumption that –9 dBV at TXI and TXQ yields +10 dBm at the final RF output. Adjacent channel power and spurious emissions are measured during constant transmission of pseudo-random data. Spectral values are characterized for the device and are not production tested on every individual part.

Table 6-3	I/Q Modulator	Characteristics	(Applies to T	XI. TXQ. and	MREF pins)
				, , , , , , , , , , , , , , , , , , ,	

Parameter	Parameter Description	Test Conditions	Min	Тур	Мах	Unit
CL	Load capacitance to AC ground				100	pF
P _{ADJ}	Adjacent channel power	Random data integrated over a \pm 40-kHz band			-39	dBV
RL	Load resistance on TXI or TXQ		1			kΩ
R _{oz}	Disabled state output impedance			25		kΩ
SE1	Spurious emissions	150 kHz ≤ freq ≤ 2 MHz 2 MHz < freq ≤ 10 MHz			-65 -79	dBV
Tdly	Absolute delay from digital input to analog output			15.1		μs
ΔV_{DC1}	Differential offset between TXI and TXQ				40	mV
ΔV _{DC2}	Differential offset between MREF and TXI or TXQ				30	mV
V _{FS}	Full scale AC output at TXI or TXQ	Digital data input is all 0s or all 1s (i.e., 18-kHz sinusoid)		0.5		Vac
V _{MREF}	MREF output voltage		0.475×Vcc	0.5×Vcc	0.525×Vcc	Vdc
Vo	Output level at TXI or TXQ	Driving full scale sinusoid	-10	-9	-8	dBV
V _{OI} /V _{OQ}	Relative levels of TXI and TXQ	Digital data input is all 0s or all 1s	-0.5		0.5	dB

6.7 CT2 NRZ OUTPUT CHARACTERISTICS

All specifications in Table 6-4 apply to the TXI and TXQ pins in NRZ mode referenced to MREF.

Table 6-4	NRZ	Output	Characteristics
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Parameter	Parameter Description	Test Conditions	Min	Тур	Мах	Unit
V _{MREF}	MREF output voltage		0.475×Vcc	0.500×Vcc	0.525×Vcc	Vdc
V _{OH}	Output High level	Referenced to MREF	0.475	0.500	0.525	V
V _{OL}	Output Low level	Referenced to MREF	-0.475	-0.500	-0.525	V

6.8 RESET

Table 6-5 refers to Figure 6-1. The parameter $t_{\rm H}$ assumes the active oscillation on the MXTAL1 pin.

Table 6-5 Reset Timing

Parameter Name	Parameter Description	Min	Тур	Max	Units
t _H	TRI1 hold after reset, in presence of MXTAL1 clock	4.0			ms
t _{RL}	Reset pulse width (Low): input	100			μs
	output		1.78		ms

Figure 6-1 Reset Timing



6.9 MICROCONTROLLER AND ADDRESS DECODER SWITCHING CHARACTERISTICS

Table 6-6Microcontroller (80C32T2) and Address Decoder Switching Characteristics
All units are in nanoseconds unless otherwise specified.

#	Parameter	Parameter Description	Variable Clock Rate Min	Variable Clock Rate Max	9.216 MHz Min	9.216 MHz Max
t1	1/TCLCL	CPUCLK Frequency	0 MHz	9.216 MHz		
t2	TLHLL	ALE Pulse Width	2TCLCL-40		177	
t3	TAVLL	Address Valid to ALE Low	TCLCL-55		53	
t4	TLLAX	Address Hold After ALE Low	TCLCL-35		73	
t5	TLLIV	ALE Low to Valid Instruction In		4TCLCL-100		334
t6	TLLPL	ALE Low to PSEN Low ⁽¹⁾	3TCLCL-40		68	
t7	TPLPH	PSEN Pulse Width ⁽¹⁾	2TCLCL-45		280	
t8	TPLIV	PSEN Low to Valid Instruction		3TCLCL-105		220
t9	ΤΡΧΙΧ	Input Instruction Hold after PSEN	0		0	
t10	TPXIZ	Input Instruction Float after PSEN		TCLCL-25		83
t11	TAVIV	Address to Valid Instruction In		5TCLCL-105		437
t12	TPLAZ	PSEN Low to Address Float ⁽¹⁾		2TCLCL+10		10
t13	TRLRH	RD Pulse Width	6TCLCL-100		551	
t14	TWLWH	WR Pulse Width	6TCLCL-100		551	
t15	TRLDV	RD Low to Valid Data In		5TCLCL-165		377
t16	TRHDX	Data Hold After RD	0		0	
t17	TRHDZ	Data Float After RD		2TCLCL-70		147
t18	TLLDV	ALE Low to Valid Data In		8TCLCL-150		718
t19	TAVDV	Address to Valid Data In		9TCLCL-165		811
t20	TLLWL	ALE Low to RD or WR Low	3TCLCL-50	3TCLCL+50	275	375
t21	TAVWL	Address Valid to \overline{RD} or \overline{WR} Low	4TCLCL-130		304	
t22	TQVWX	Data Valid to WR Transition	TCLCL-60		48	
t23	TQVWH	Data Valid to Write High	7TCLCL-150		609	
t24	TWHQX	Data Hold After WR	TCLCL-50		58	
t25	TRLAZ	RD Low to Address Float		0		0
t26	TWHLH	\overline{RD} or \overline{WR} High to ALE High	TCLCL-40	TCLCL+40	68	148
t27	TRWCS	\overline{RD} or \overline{WR} High to \overline{CS} High	TCLCL-30	TCLCL+10	78	118

Note:

These parameters behave differently for the 9.216-MHz clock rate than for slower clock rates for power consumption considerations. Values listed under the Variable Clock Rate columns apply to all CPUCLK rates other than 9.216 MHz.



Figure 6-2 Microcontroller External Program Memory Read Cycle



17673A-013





17673A-014

6.10 CT2 FORMATTER SWITCHING CHARACTERISTICS

Figure 6-5 shows timing of the TXEN, RXEN, and SHCTR signals, relative to the receive and transmit data. Values are tabulated for the various multiplexes in Table 6-7. One bit period is nominally 13.89 μ s (1/72 kHz).

Figure 6-5 RF Interface Control Signal Timing



Table 6-7 RF Interface Control Signal Timing

All values are typical. (T_{MDM} = modem delay measurement adjustment)

Parameter	Description	MUX1.2, MUX2	MUX1.4	MUX3
t _{IQD}	I/Q modulation delay	15.1 μs	15.1 μs	15.1 μs
t _{RD}	Receive data length	66 bits	68 bits	CPP: 288 bits CFP: N/A
t _{RRL}	End of valid data to RXEN Low	6.9 μs	6.9 μs	N/A
t _{RTD}	Receive data to transmit data	CFP: 6.5 –T _{MDM}	CFP: 4.5 –T _{MDM}	CFP: 6.5 –T _{MDM}
		CPP: 5.5 – T _{MDM}	CPP: 3.5 –T _{MDM}	CPP: 5.5 –T _{MDM}
t _{SHD}	SHCTRL High to receive data	7.8 μs	7.8 μs	7.8 μs
t _{SRL}	SHCTRL Low to RXEN Low	6.9 μs	6.9 μs	6.9 μs
t _{SWT}	ANTSW High to TXEN High	6.9 μs	6.9 μs	6.9 μs
t _{TD}	Transmit data length	66 bits	68 bits	CPP:720 bits
t _{TRD}	Transmit data to receive data	CFP: 5.5 + T _{MDM}	CFP: 3.5 + T _{MDM}	CFP: 5.5+T _{MDM}
		CPP: 6.5 + T _{MDM}	CPP: 4.5 + T _{MDM}	CPP: 6.5+T _{MDM}
t _{TRH}	End of transmit data to RXEN High	11.3-87.6 μs	11.3-87.6 μs	11.3-87.6 μs
		49.5 μs (default)	49.5 μs (default)	49.5 µs (default)
t _{TTD}	TXEN High to valid transmit data	0.868-32.1 μs	0.868-32.1 μs	0.868-32.1 μs
		4.3 μs (default)	4.3 μs (default)	4.3 μs (default)
t _{TTL}	End of data to TXEN Low	4.3-36.0 μs	4.3-36.0 μs	4.3-36.0 μs
		42.5 μs (default)	42.5 μs (default)	42.5 μs (default)

6.11 500-Hz CT2 SYNC PLL CHARACTERISTICS

The performance values listed in Table 6-8 are characterized for the device and are not production tested on every part. All frequency values are referenced to the MXTAL1 frequency reference (i.e., 18.432 MHz / 36864).

Trackable input jitter J_{IN} is the jitter to which the PLL can respond immediately by tracking. Jitter input exceeding J_{IN} will be filtered so that the PLL response will not exceed the rail.

Tolerable input drift Δ Fin is a frequency difference relative to the MXTAL1 pin reference frequency to which the PLL can respond immediately by tracking. Input drift exceeding Δ Fin is not guaranteed to be tracked. The tracking range is limited by Rail so that in cases of extremely high Δ Fin, the PLL will pull only as far as the Rail value.

Parameter	Description	Min	Тур	Max	Units
Fin	Input frequency		500		Hz
ΔFin	Tolerable input drift assuming no input jitter	-150		+150	ppm
J _{ADJ1}	Output adjustment rate per bit	-108		+108	ns per 9 bits
J _{ADJ2}	Output adjustment rate per frame	-432		+432	ns per CT2 frame
J _{IN}	Trackable input jitter, assuming no input drift		±432		ns
Rail	PLL tracking limit		±200		ppm
t _{SPW}	Input minimum pulse width High or Low	1			μs

 Table 6-8
 Synchronization PLL Characteristics

6.12 PCM PORT SWITCHING CHARACTERISTICS

6.12.1 Slave Mode 8-kHz Frame Sync Characteristics

CLK8K appears on the BDP3_OUT5 pin when appropriately programmed in BDMUX[6:5] and enabled in MECTR1[4]. The relationship to the 500-Hz SYNC is demonstrated in Figure 6-6. CLK8K aligns with either the rising or falling edge of SYNC, as programmed in BSYNC[5]. Table 6-9 tabulates timing parameters.

Figure 6-6 500-Hz SYNC-CLK8K Relationship



 Table 6-9
 8-kHz Frame Synchronization Timing Parameters

Parameter	Description	Min	Тур	Max	Units
t _{CPW}	CLK8K pulse width	62.39	62.50	62.61	μs
t _{JOUT}	Output jitter on CLK8K, assuming no jitter on input SYNC	-165		+165	ns
t _{SPW}	SYNC input pulse width	1			μs
6.12.2 A-law/µ-law Format Switching Characteristics



Figure 6-9 A-law/µ-law PCM Port Receive Timing



Table 6-10A-law/ μ -law PCM Port Timing Parameters

Parameter	Description	Min	Тур	Max	Units
f _D	PCMCLK data clock frequency	64		2048	kHz
1/f _D	PCMCLK data clock period	488 ns		15.63 μs	
t _{HD}	Hold for PCMIN after falling PCMCLK edge.	50			ns
t _{OD}	Output delay from TE High and PCMCLK rising edge to valid data		20		ns
t _{oz}	Output delay to high impedance state after TE is (goes) Low and PCMCLK is (goes) High.		20		ns
t _{PW}	PCMCLK pulse width, High or Low	50			ns
t _{SUD}	Setup for PCMIN before falling PCMCLK edge.	100			ns
t _{SUE}	Setup for enables RE and TE before rising edge of PCMCLK	-50		+50	ns

6.13 B CHANNEL ADPCM PORT SWITCHING CHARACTERISTICS





Table 6-11 B Channel ADPCM Port Timing

(all units in ns)

Parameter	Description	Minimum	Maximum
t _{DD}	BCLK Low to output data valid	0	100
t _{DH}	Input data hold after BCLK High	0	
t _{DS}	Input data setup to BCLK High	150	

6.14 SERIAL PORT SWITCHING CHARACTERISTICS

Table 6-12 Serial Port Switching Characteristics

(all units in ns)

Parameter	Description	Minimum	Maximum
t _D	SCLK Low to output data valid	0	100
t _H	Input data hold after active SCLK edge	0	
t _{SU}	Input data setup to active SCLK edge	150	

Figure 6-11 Serial Port Timing (SIOMODE[2] = 0)



Figure 6-12 Serial Port Timing (SIOMODE[2] = 1)





7.1

PACKAGE DIMENSIONS

PQR 100 PQFP TRIMMED AND FORMED LEAD

Metric, Rectangular, Trimmed and Formed (excised from Molded Carrier Ring) (all measurements in millimeters)



1. All measurements are in millimeters unless otherwise noted.

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2. Not to scale; for reference only.

Package Dimensions

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PQR 100 PQFP Trimmed and Formed Lead (continued)



pqr100 4-15-94

7.2 **PQR 100 PQFP WITH MOLDED CARRIER RING**

Metric, Rectangular, with Molded Carrier Ring



